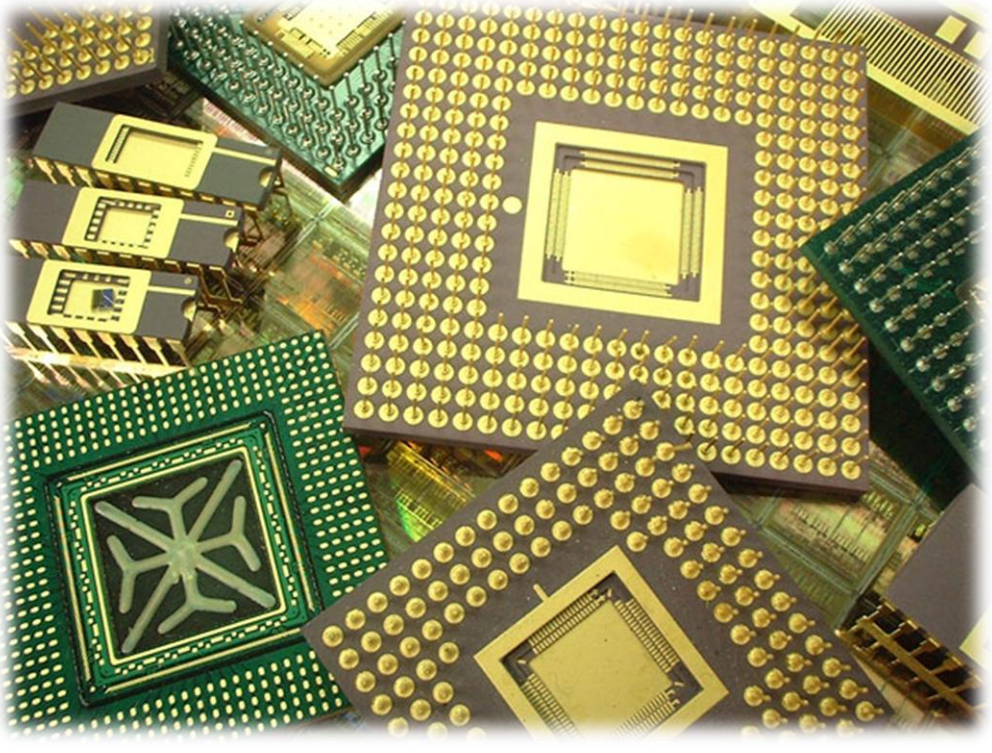
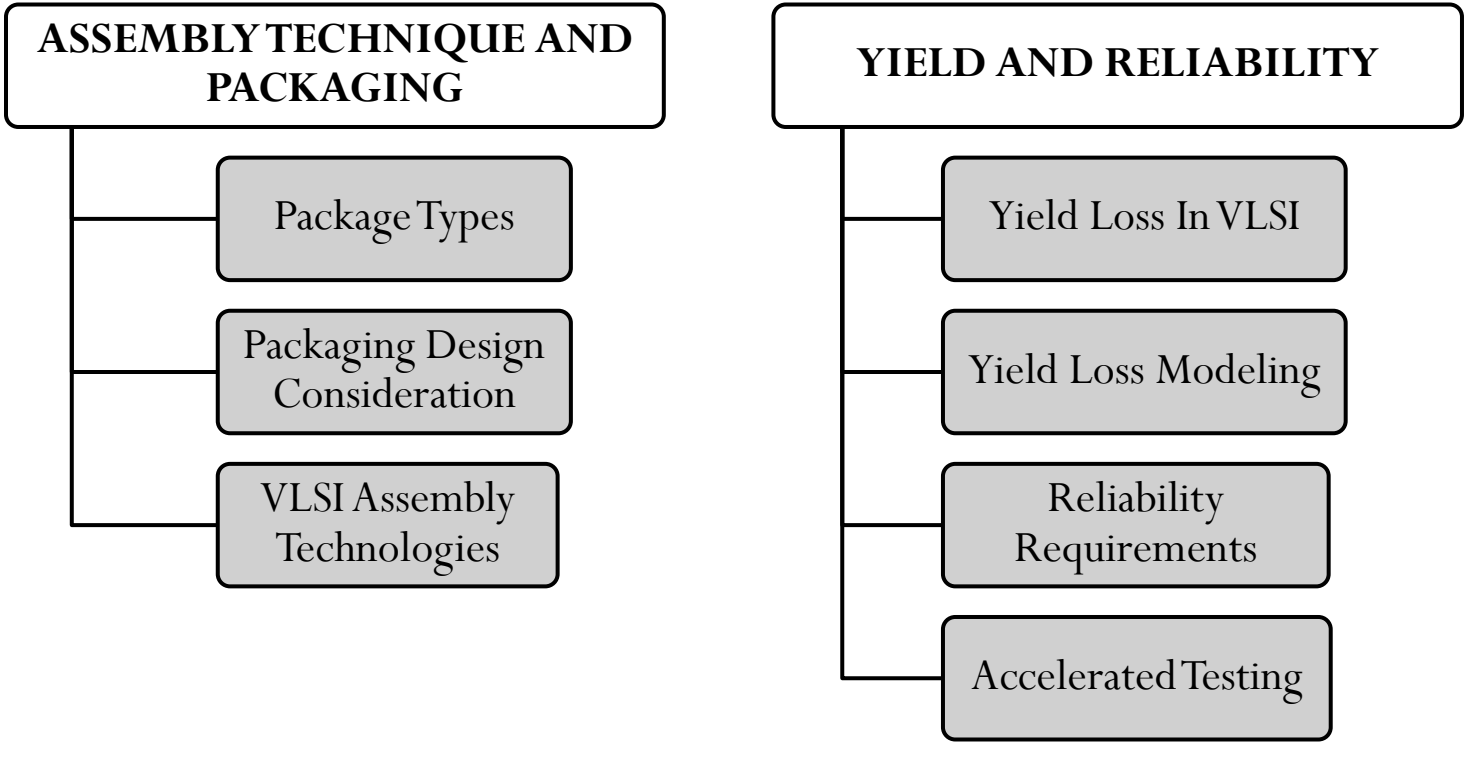


# UNIT V

# Syllabus


ASSEMBLY TECHNIQUE AND PACKAGING
Package Types
Packaging Design Consideration
VLSI Assembly Technologies
YIELD AND RELIABILITY
Yield Loss In VLSI
Yield Loss Modeling
Reliability Requirements
Accelerated Testing

# ASSEMBLY TECHNIQUE AND PACKAGING

a. Package Types
b. Packaging Design Consideration
c. VLSI Assembly Technologies

# Introduction

- The packaging of VLSI die or chip is required to provide electrical connection and mechanical & environmental protection.
- The packaging of VLSI die affects the overall cost, performance and reliability of the packaged die.
- The number of I/O terminals required for logic gate and microprocessor devices increases continuously with number of gates on the chip.

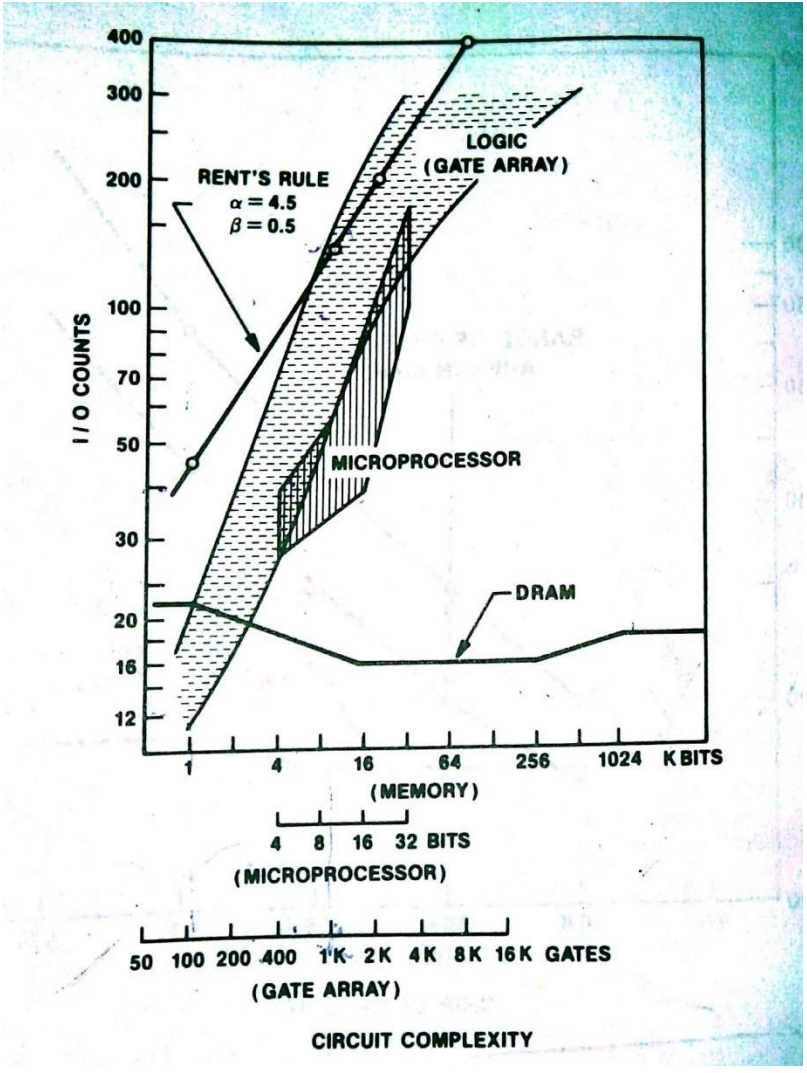
# Contd...

- According to the **Rent's Law** the number of signal terminals or packages I/Os required for logic device is given by:

$$\text{Number I/O} = \alpha(\text{Gate Count})^{\beta}$$

- Where $\alpha$ and $\beta$ are coefficients.
- See figure; it compares the I/O demands placed on packaging by logic and microprocessors.

**Figure** : Circuit complexity Comparison of I/O requirement for logic, microprocessor and memory devices (DRAM) as a function of circuit complexity [S M Sze Page 568]



# Contd...

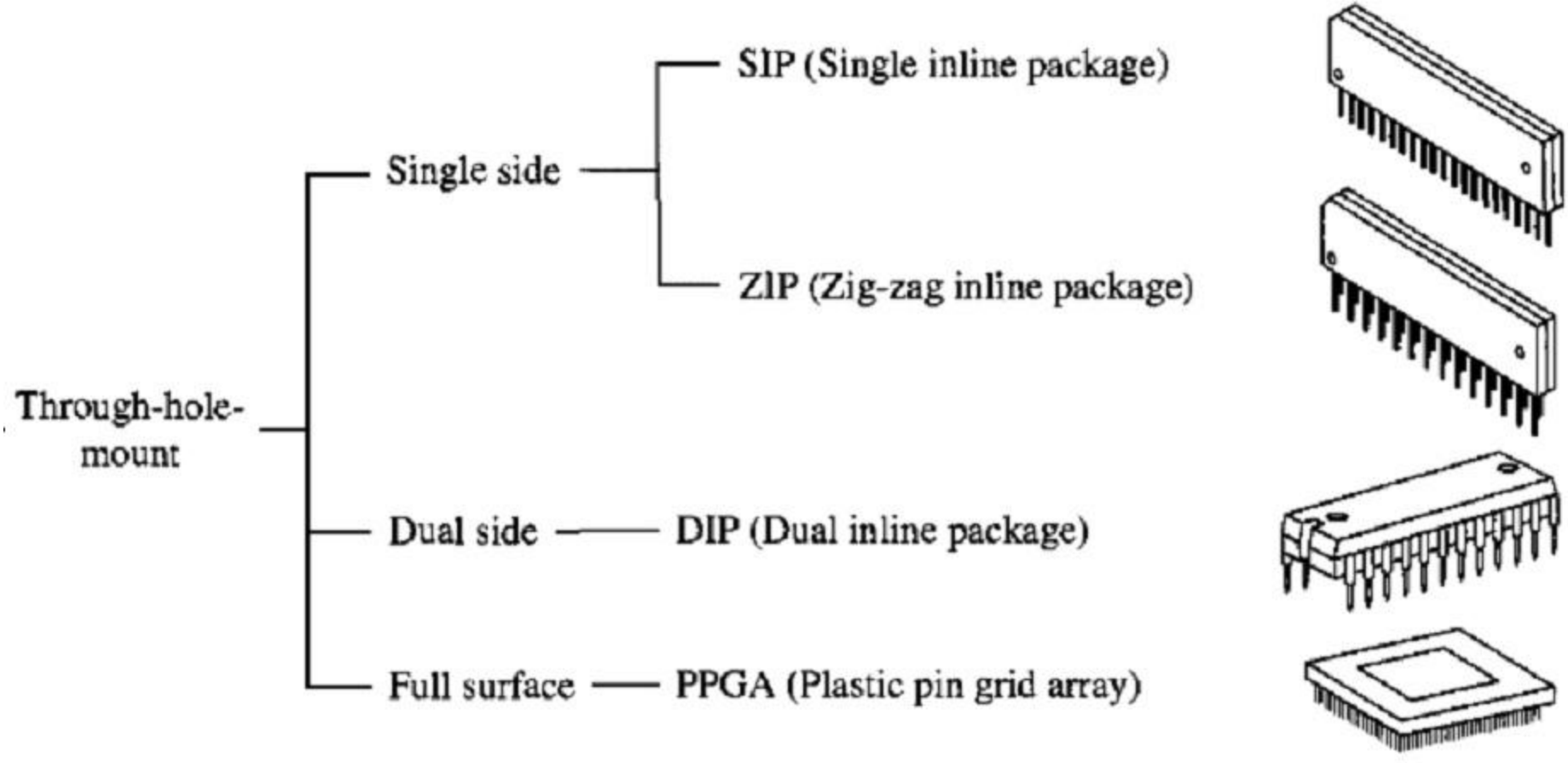
- Since the silicon feature size is continuously decreasing so I/O count, number of interconnections and package pins are increasing.
- The package design will need to provide good heat dissipation, good electrical performance and high reliability.

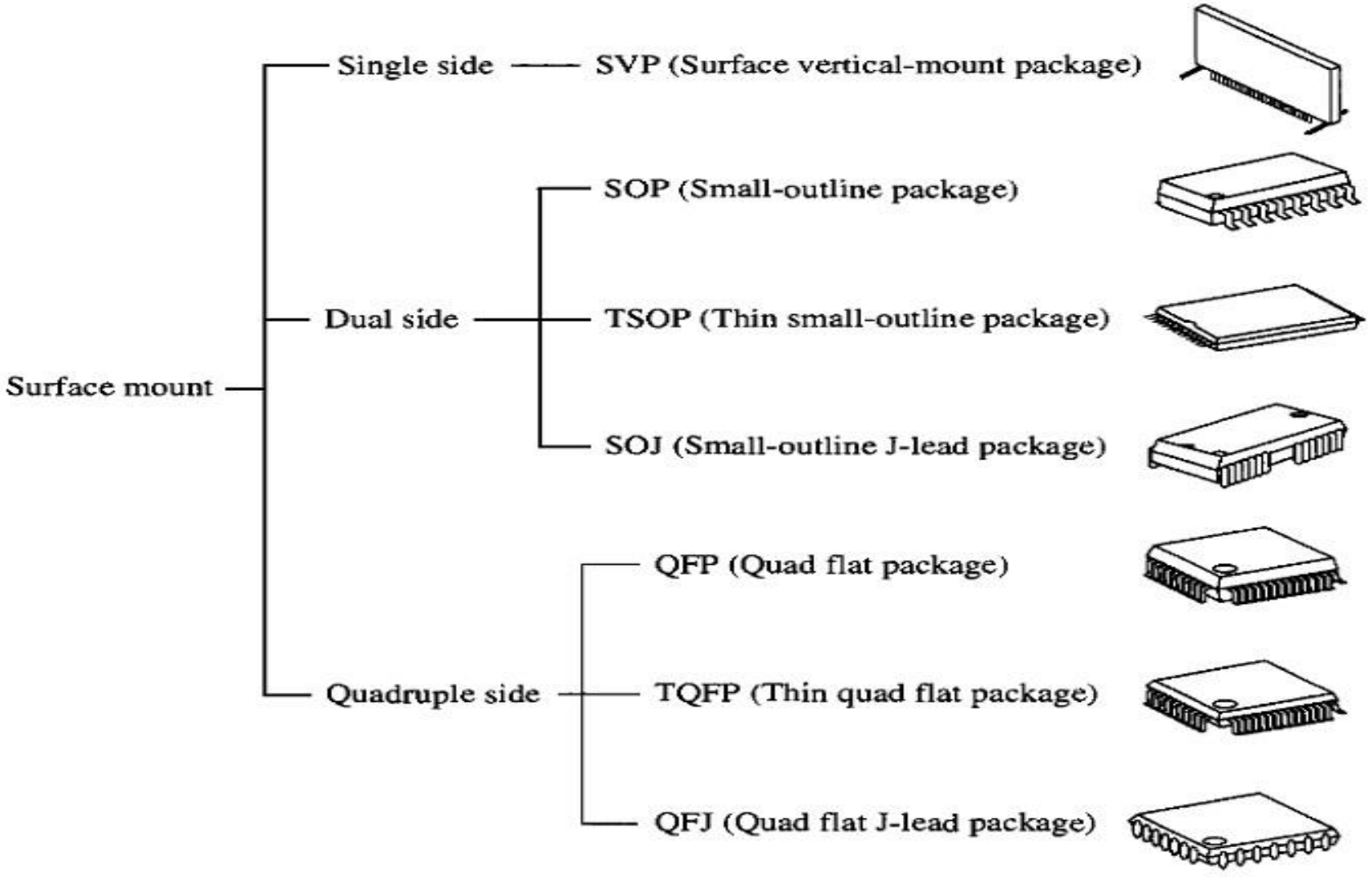
# Problem

- Estimate the number of gates that can be included on a logic gate array chip which is to be assembled in a 100 I/O package. Assume $\alpha = 4.5$ and $\beta = 0.5$
- Ans = 493 gates.

# Package types

- Lot of packages types are available in VLSI both for through hole mounting and surface hole mounting to PWBs (Printed Wiring Board).
- The through hole (TH) includes the Dual in line (DIP) and pin grid array (PGA), with pins from 8 to 300.
- Both the types of mounting packages are available in ceramic and plastic types.
- Packages leads are usually on 2.54 mm pitch.
- The SM packages I/Os up to 28 terminals are DIP and known as small outline (SO), are available in plastic packages.

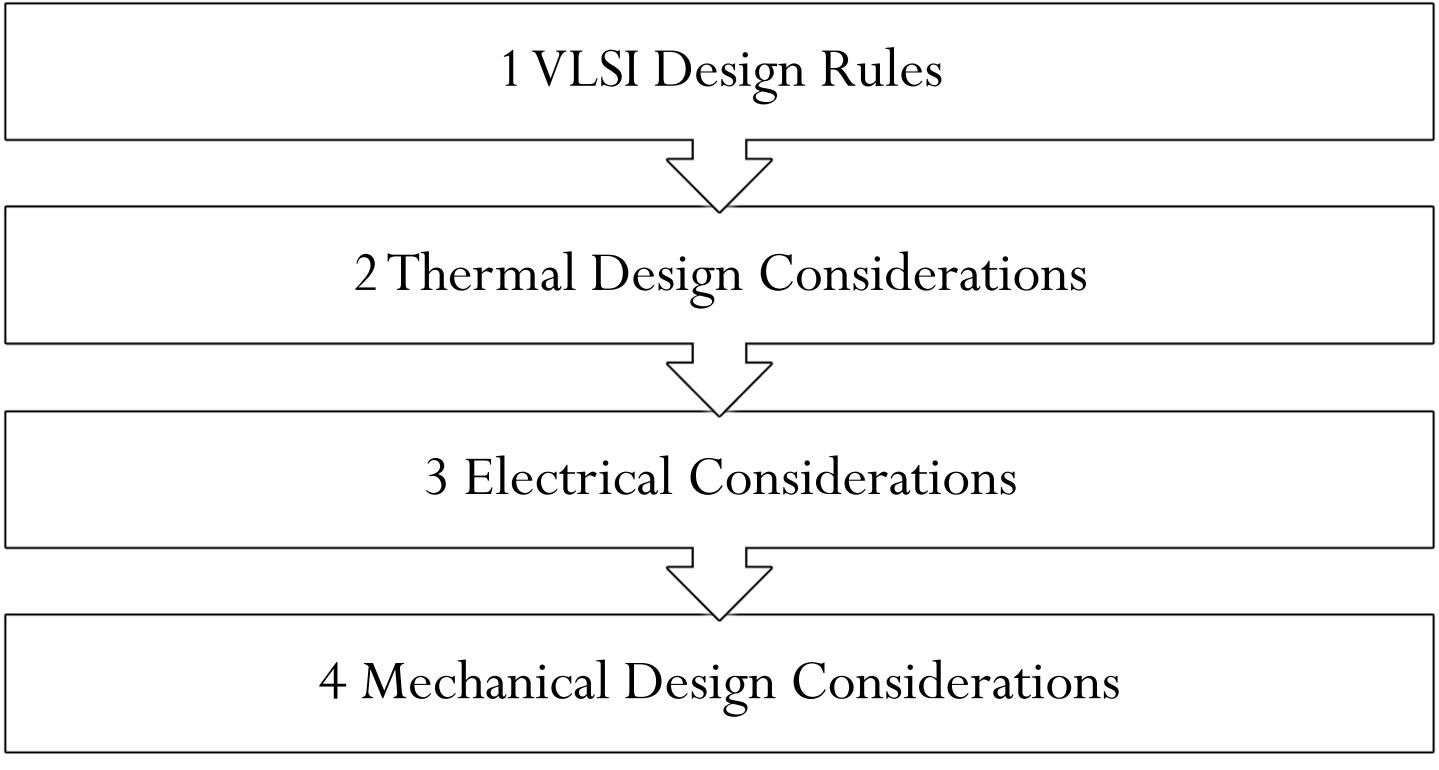

Through-hole-mount
Single side
SIP (Single inline package)
ZIP (Zig-zag inline package)
Dual side
DIP (Dual inline package)
Full surface
PPGA (Plastic pin grid array)


Surface mount
Single side
SVP (Surface vertical-mount package)
Dual side
SOP (Small-outline package)
TSOP (Thin small-outline package)
SOJ (Small-outline J-lead package)
Quadruple side
QFP (Quad flat package)
TQFP (Thin quad flat package)
QFJ (Quad flat J-lead package)

# Contd...

- The quad type are known as chip carries (CC) and flat packs, both available in ceramic and plastic packages.
- All SM quad types packages are available in ceramic and plastic packages.
- Ceramic based, hermetically sealed packages are designed for high performance.
- There are lot of other packages, i.e., DIP, single in line packages (SIP), zigzag in line packages (ZIP) etc.

# Packaging Design Consideration



# 1. VLSI Design Rules

- In order to achieve high yields in VLSI package assembly establishment of good chip design rules is essential.
- Rules must be different for particular package type.
- The rules must be compatible with assembly equipment.
- As the I/O count grows and the active VLSI device size shrinks, the bonding pad size and spacing (pitch) should be reduced.
- Figure shows consequence of increasing I/Os on the bonding pad pitch for several chip sizes.
- Reliability and the ability to assemble VLSI chips is affected by the chip layout.

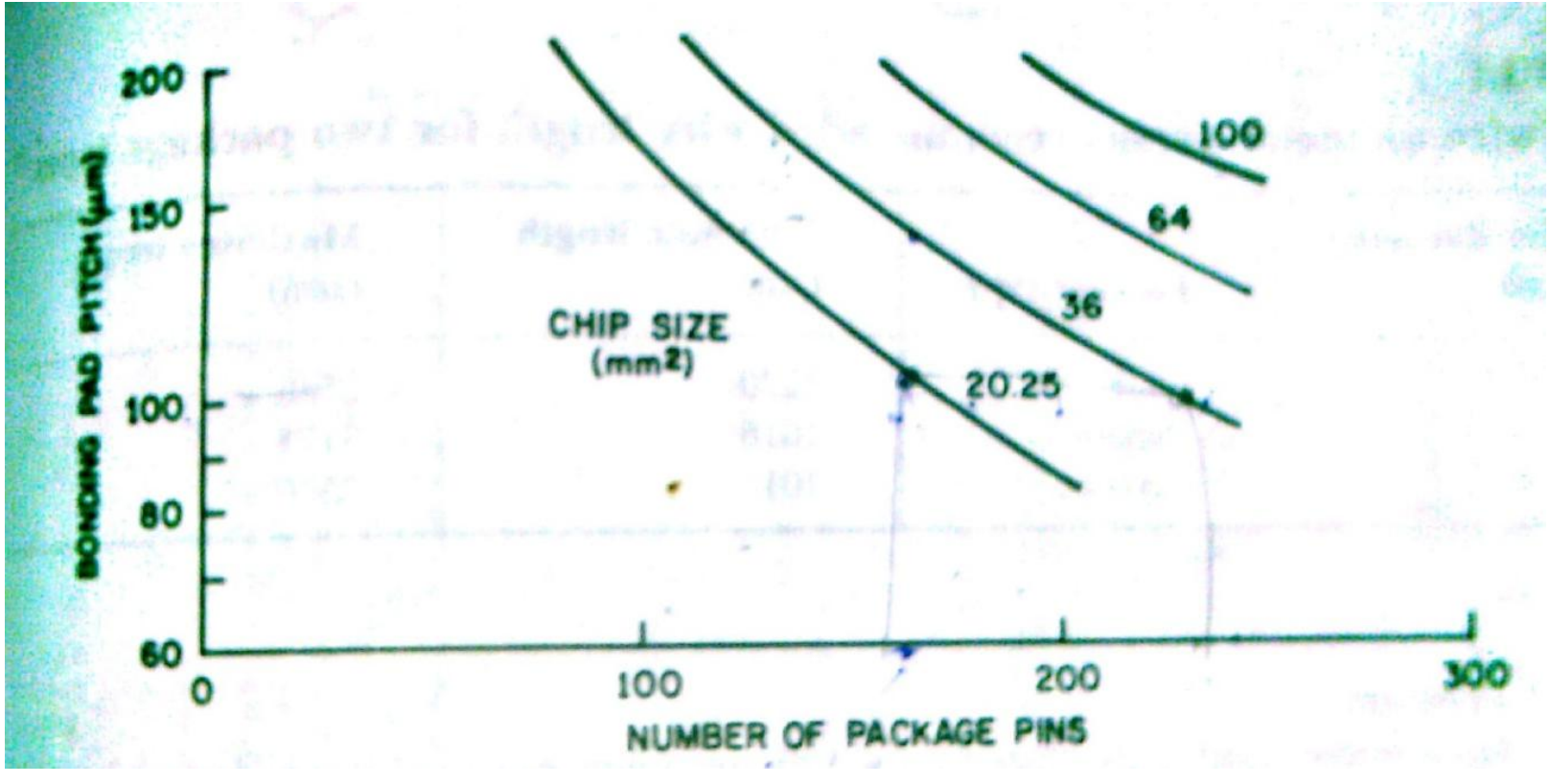



Figure: Bonding pad pitch versus chip lead count for several chip sizes. [S M Sze page 573]

# 2. Thermal Design Considerations

- The operating junction temperature of a silicon die must be as low as possible to prevent the failure rates.
- The heat is transferred from die to surface of the package (case) by conduction and from the package to the ambient by convection and radiation.
- Usually the temperature difference between the case and ambient is small so the radiation can be neglected.
- The packaged device environment must be established for the following variables.

PWB Temperature

Total power dissipation on the board

Local neighbor power dissipation

Conductivity of the PWB

# Contd...

- The overall thermal resistance can be considered as the sum of two thermal resistance components $\theta_{jc}$ and $\theta_{ca}$, where

$$\theta_{ja} = \theta_{jc} + \theta_{ca} \ (^0\text{C/Watt})$$

$$\theta_{jc} = [T_j - T_c]/P$$

$$\theta_{ca} = [T_c - T_a]/P$$

# Contd...

- Where
  - $\theta_{ja}$ = junction to ambient thermal resistance
  - $\theta_{jc}$ = junction to case thermal resistance
  - $\theta_{ca}$ = case to ambient thermal resistance
  - $T_j$ = average die or junction temperature ($^0$C)
  - $T_c$ = average case temperature ($^0$C)
  - $T_a$ = ambient temperature ($^0$C)
  - P = power (Watts)

# Contd...

- Thermal characterizations are done by mounting the package device as shown in figure.

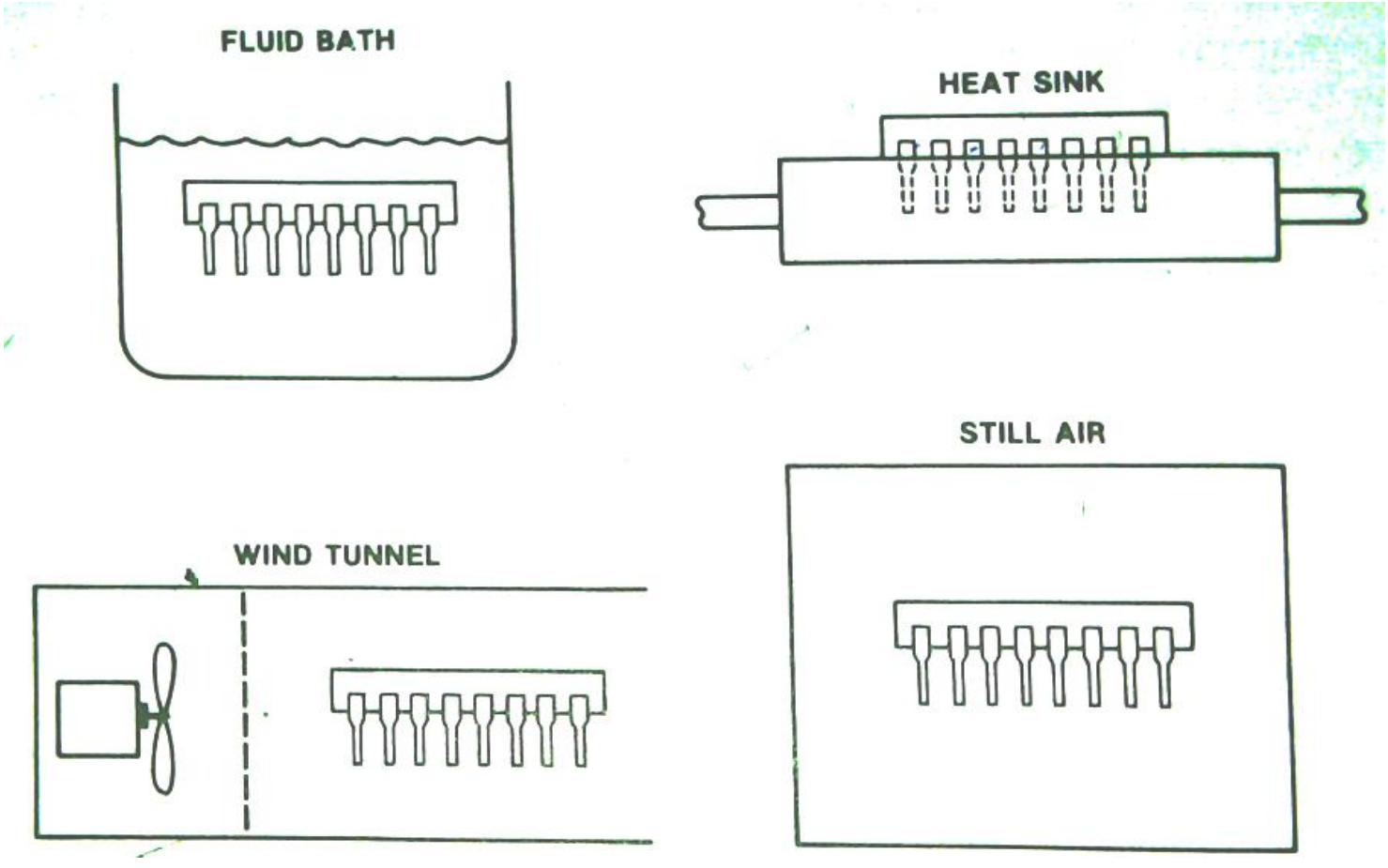



Figure : Typical package-mounting arrangements for thermal characterization

# Problem [S M Sze]

- What is the junction to ambient thermal resistance for a device dissipating 550 mW into an ambient of 70 $^0$C and operating at a junction temperature of 125 $^0$C.
- Answer: 100 $^0$C/W.

# 3. Electrical Considerations

- In IC packaging level, there are several electrical performance criteria.
  - Low ground resistance (minimum power supply voltage drop)
  - Short signal leads (minimum self inductance)
  - Minimum power supply spiking due to signal lines simultaneously switching
  - Short paralleled signal runs near a ground plane (minimum capacitive loading)
  - Maximum use of matched impedances to avoid signal reflection.

# Contd...

- All of the avobe criteria depends upon some variables such as;
  - conductor cross section
  - conductor length
  - dielectric thickness
  - dielectric constant of packaging body.
- The most important electrical consideration in IC packaging is noise reduction.
- When a line switches the voltage induced in the ground line is given be;

$$V_i = L_g \, di/dt$$

- Where
  - $V_i$ is induced voltage
  - $L_g$ is the inductance of the ground lead
  - di/dt is the derivative of the current with respect to time.

# Contd...

- If j lines are switching, then $V_i$ is given by;

$$V_i = L_g \sum di_j/dt$$

- So in order to reduce $V_i$ multiple grounds must be used to reduce $L_g$.
- If m ground leads are used, the total inductance will be $L_g/m$.
- The inductance can be reduced through the use of large ground planes within the package.

# 4. Mechanical Design Considerations

- The material for package construction ideally match physical properties of the VLSI die usually TCE (Thermal Coefficient Expansion).
- In actual design, the die is attached using materials like solder, alloy or adhesive.
- During the packaging process the heat may melt solders.
- So Alloy 42 (Fe-Ni 42%) is used, it has poor thermal conductivity, but closely matches the TCE of silicon.
- Mechanical reliability requires a good matching between the thermal properties like the TCE of the integrated circuit and the package.
- Hermetic packages offer high degree of matching, because no package materials comes in direct contact with IC surface.

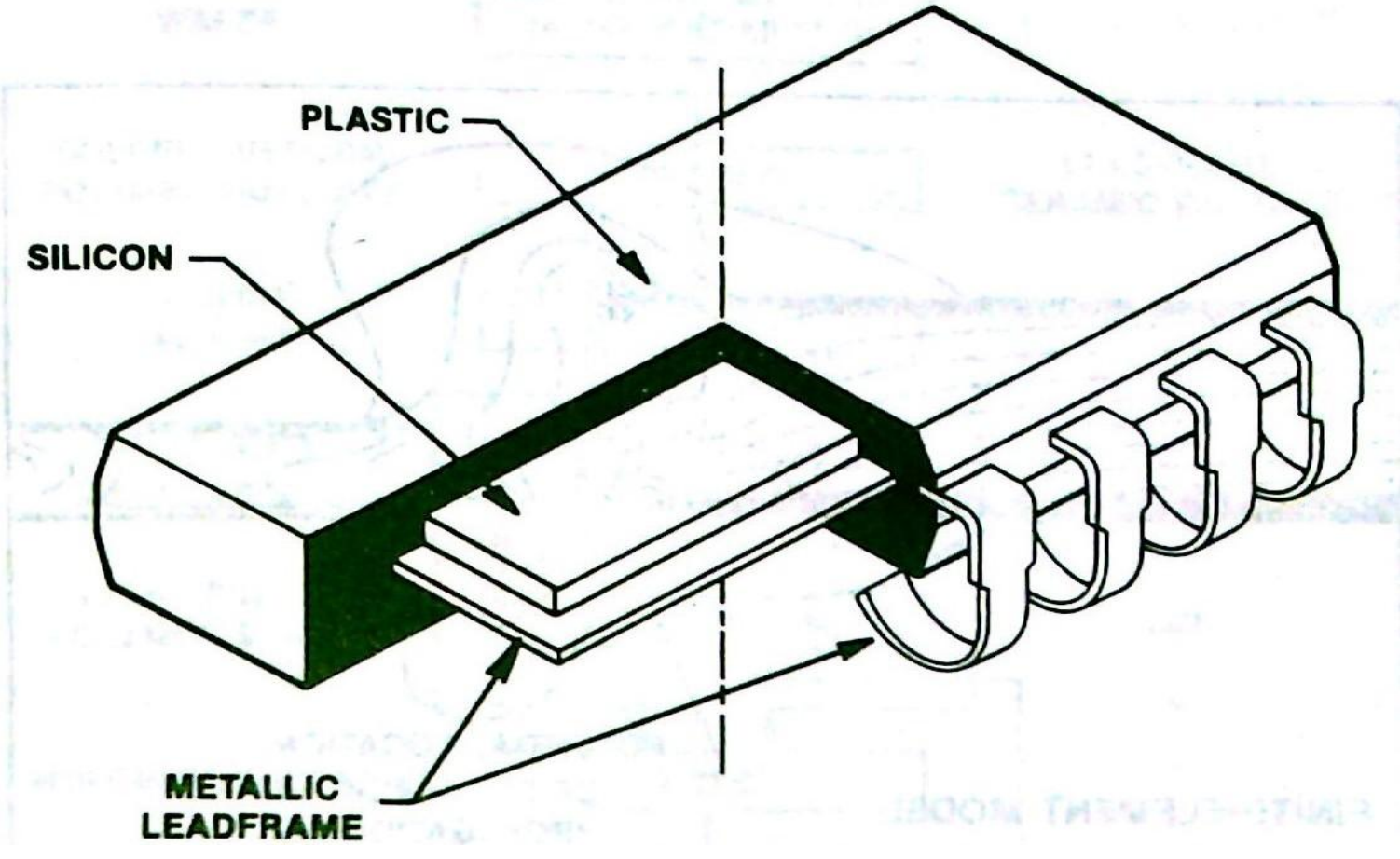



Figure: The plastic package (Hermetic Type)

# VLSI Assembly Technologies

- Process of electrically connecting I/O bond pads on the IC.
- It enables an IC to be electrically interconnected to the package.
- The **first step** is the preparation of the wafer.
- The **second step** is the die attach. In this step the die is attached to the package.
- The **third step** is the wire bonding, which is the process of connecting the bond pad to the lead of the package.

# Contd...

- The **fourth step** is to encapsulate the die. In this step the die is closed from the interference of external contaminant and protecting from damage etc.
- The **fifth step** is to seal the package.
- The **sixth step** is Molding in which the device is encapsulated in plastic material.
- The **last step** is to test the packaged device.

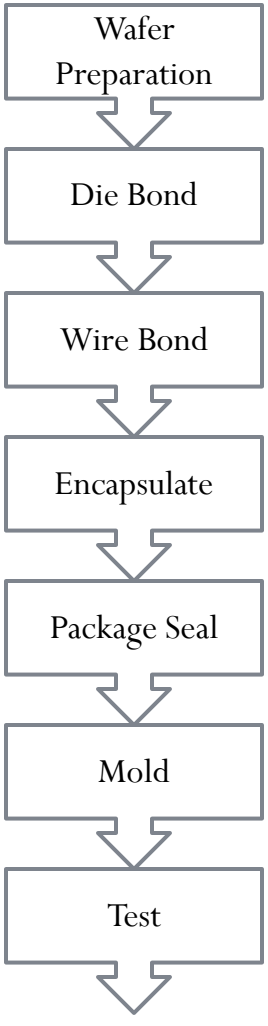



Figure: Generic assembly sequence for plastic and ceramic packages

# Wafer Preparation

- The silicon crystal obtained after Cz process is called “ingot”.
- The shaping operation removes the seed and tang ends from the ingot.
- The ingot surface is then grounded throughout to an exact diameter.
- Once the ingot surface is made smooth, ingot is sliced in wafers by high speed “diamond saw”.
- Slicing is done by inner diameter sawing using a diamond saw.
- It is rotated at a high speed and then moved across the ingot to obtain wafer slices.
- Slicing is done very slowly.
- Thicker wafers are usually preferred.
- After slicing there is a variation in the thickness of the sliced wafer.

# Contd...

- So, it can't be used directly for IC fabrication.
- Lapping is done in order to remove the cracked or damaged surface of the wafer.
- After lapping edge grinding takes place.
- Etching is the process of selectively removing unwanted semiconductor material from the wafer.
- Wet etching: chemical solution (mixture of HF & $HNO_3$) is used.
- Dry Etching: sputtering method is used.
- The purpose of polishing is to provide smooth surface of the wafer.
- The wafer surface is polished to mirror like finish.

# Contd...

- Wafers are cleaned and dried for use in IC fabrication.
- The final wafer thickness is about one third of the sliced wafer.
- Thickness of the fabricated wafer is normally around 650 μm.
- It needs to be thinned before the assembly begins.
- The thinning is necessary to reduce thermal stress due to mismatch of the thermal coefficient of expansion (TCE) between the silicon die and the packaging material.

# Contd...

- Different color inking schemes may be adopted to distinguish between commercial/industrial die and military die.
- One of the schemes is to ink the die with green color for commercial/industrial die, no color is to be used for military, and red color for fail die.

# Die Attach

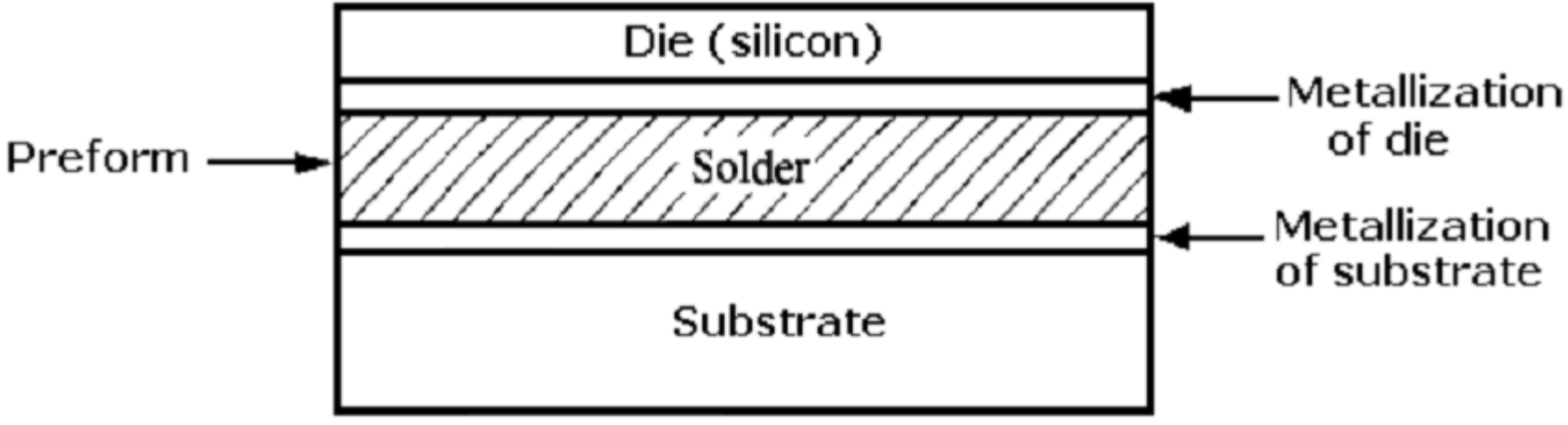
- It is a process of attaching the die permanently to package.
- Die attachment process requires of high temperature and cooling down to room temperature.
- Material that has TCE close to that of silicon crystal is preferred in package construction.
- Packaging materials that has TCE as that of silicon reduces thermal stress.
- In real situation, there is no such material that can provide perfect match with the silicon.
- However, Alloy 42 (42% nickel-58% iron) lead frame are used due to close TCE match for hermetic-ceramic package and plastic package.

# Contd...

- There are basically 2 techniques for die attach.
  A. **Eutectic Die Attach**
  B. **Epoxy Die Attach**

# A. Eutectic Die Attach

- Eutectic is made from the Greek word "eutecsis", which means (eu = easy) and (tecsis = melting).
- In Eutectic die attach the die is metallurgically attached to package with the material typically made from Alloy 42.
- After that the material (preform) melts and reacts with silicon to form an Au-Si composition bond between the backside of the die and the substrate (package) of the ceramic.




The basic structure of a silicon device die attach with a metal preform

# B. Epoxy Die Attach

- Silver filled epoxy adhesive is used for die attach.
- Epoxy is a strong adhesive used for sticking things together and covering surfaces.
- In VLSI assembly, epoxy is fed onto the substrate material to ensure the required bond line thickness is created avoiding void.
- The process time of epoxy die attach usually is 1 to 2 seconds at room temperature.

# Wire Bonding

- Wire bonding is the most common method for connecting the bond pads on the die to the package.
- Aluminum or gold wires of diameter 25 to 30 μm are usually used because they bond well to the bond pads on the die and the package.
- The temperature of wire bonding ranges from 150 $^0$C to 250 $^0$C.

# Test

- Wafer testing is a step performed during semiconductor device fabrication.
- Testing is performed before and after wafer is sent to die preparation.
- All individual integrated circuits that are present on the wafer are tested for functional defects.
- The wafer testing is performed by a piece of test equipment called a wafer prober.

# YIELD AND RELIABILITY

a. Yield Loss In VLSI
b. Yield Loss Modeling
c. Reliability Requirements
d. Accelerated Testing

# Introduction

- There are two conditions that must be satisfied in order for a VLSI to be useful. These are;
  1. The fabricated circuits must be produced in large quantities at low cost.
  2. The circuits must be capable of performing their function throughout their intended life.
- So in order to produce Integrated circuits that meet these two requirements, we must have to understand the mechanisms that lead to **high cost and unreliable devices**.

# Yield Loss In VLSI

- Ideally in properly fabricated VLSI circuits, all of the circuits on the wafer must be good functional circuits.
- The yield is defined as the ratio of good chips to the total number of manufactured chips.
- The yield may be less than perfect because of the following three reasons.
  1. Processing Effects
  2. Circuit Sensitivities
  3. Point Defects

# 1. Processing Effects

- On the tested wafer, there are lot of regions with good chips and some regions with defected chips.
- Processing effect is responsible to existence of low yield chips.
- These effects may arise due to variations in the thickness of the oxide or polysilicon layers.
- Due to variations in the oxide layer, the lithographic pattern may be changed.
- The regions where the polysilicon layer is thinner than average becomes over-etched when wafer is etched for the time needed to etch the polysilicon in regions where the layer is thicker than average.
- If the channel length is too shorter due to processing effect, the transistor cannot be turned off when the appropriate gate voltage is applied.

# Contd...

- So, in this case circuit may not function well or may have excessive leakage currents.
- Variation in the doping of implanted layers can lead to variations in the contact resistance to the implanted layers.
- The stacking faults during oxidation may lead to excessive leakage current and circuit failure.
- So in order to minimize these effects one must take care during the processing of the wafer.

# 2. Circuit Sensitivities

- The threshold voltage ($V_T$) and the channel length (L) of the MOS transistor are the two most important parameter in MOS circuit.
- Variations in the gate length, source and drain junction depth may cause channel length to vary.
- So ultimately the threshold voltage will vary.
- The speed of the MOS increases with increase in threshold voltage ($V_T$) and decrease in channel length (L).
- It will lead to low yield due to sensitivity of the circuit.
- If the circuit sensitivity have been determined, circuit can be redesigned to reduce these sensitivities.
- It will produce high yield at low cost.

# 3. Point Defects

- The point defect is the region of the wafer, where the processing is imperfect.
- For example; a 3 μm diameter dust particle on the wafer can cause a break in the metal conductor.
- Similarly, a 200 μm dust particle could cause a large area of metal to be missing from the chip.
- Dust or other particle in the environment is one of the most common cause of this type of defect.
- They may present in the photoresist and deposited on wafer during the photoresist operation.
- Point defects can occur on lithographic masks as well as on silicon wafers.

# Yield Loss Modeling

- By accurately modeling the yield in terms of fundamental parameters, we can predict the cost and availability of future circuits.
- Generally yield of an IC is expressed in the form;

$$Y = Y_0 \; Y_1 \, (D_0, A, \alpha_i)$$

- Where
  - Y is the ratio of good chips per wafer to the total number of chips per wafer.
  - $(1-Y_0)$ is the fraction of chip sites that yield bad chips either due to the processing effects or because of the circuit sensitivities.
  - $(1-Y_1)$ is the fraction of the remaining chip that yield bad chips due to point defects.
  - $D_0$ is the density of point defect per unit area.
  - A is the area of the chip.
  - $\alpha_i$ is the parameter depends upon the model of the yield.

# Contd...

- Yield modeling can identity those processes and mechanisms that limit the yield of an IC.
- Once the yield limiting features are identified, the processes can be improved or eliminated.
- For example projection printing has replaced contact printing to reduce defect density.
- Dry etching has replaced wet etching to control better feature size.
- Ion implantation has replaced diffusion to better control of resistance, junction depth and threshold voltage.
- The yield modeling is the tool for improving the generation, processes and designs.

# Contd...

- There are basically following yield loss modeling ;
  1. Uniform Density of Point Defects
  2. Simple Nonuniform Distributions of D
  3. The Gamma Distribution of D
  4. Yield of Chips with Redundant Circuitry
  5. Multiple Types of Defects
  6. Radial Distribution of Defects

# 1. Uniform Density of Point Defects

- The yield loss in IC other than processing effects and circuit sensitivities may be due to randomly distributed point defects.
- Figure shows 24 chip sites with 10 defects randomly distributed over the area.
- In this figure; 16 out of 24 sites have no defects, so they are good chips.
- On the remaining 8 sites 6 have 1 defect and 2 have 2 defects.
- No site have more than 2 defect.
- If n defects are distributed randomly among N chips, the probability $P_k$ that a given chip contains k defects is given by the binomial distribution

$$\mathrm{Pk} = \frac{n!}{k!\,(n-k)!} \cdot \frac{1}{\mathrm{N}^{\mathrm{n}}} (\mathrm{N}-1)^{\mathrm{n-k}}$$

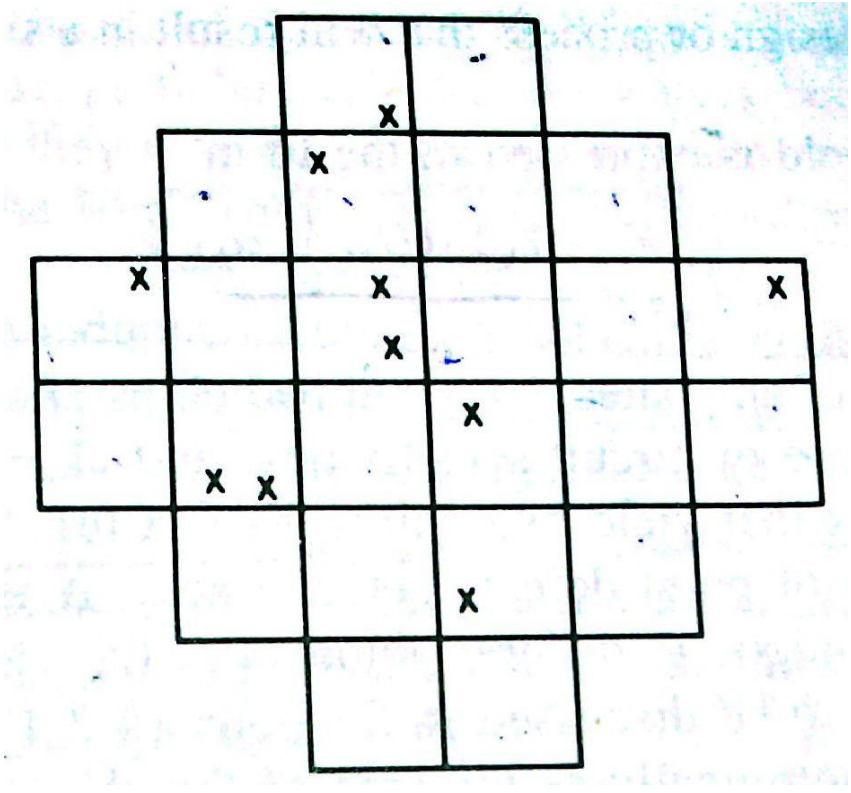


Fig: an array of 24 chip sites with 10 defects (indicated by x) randomly distributed on the sites

# Contd...

- The binomial distribution can be approximated by the more tractable Poisson distribution

$$P_k \cong e^{-m}\frac{m^k}{k!}$$

- The probability that a chip contains no defect, which is yield, is given by;

$$Y_1 = P_0 = e^{-m}$$

- And the probability that a chip contains one defect is given by;

$$P_1 = me^{-m}$$

# Contd...

- If the area of the chip is A, the total usable area in the wafer will be NA, and the density of defects is $n/NA = D_0$.
- The average number of defects per chip m is,

$$m = \frac{n}{N} = \frac{D_0 NA}{N} = D_0 A$$

- And

$$Y_1 = P_0 = e^{-D_0 A}$$

- The poisson estimate of the yield of good chips can be used to predict the yield during the early manufacture of ICs.

# 2. Simple Nonuniform Distributions of D

- In this case, the yield of chips on a wafer can be expressed as;

$$Y = \int_0^{\infty} e^{-D_0 A} f(D) dD$$

- Where $D_0A$ is nonuniform across the wafer & $f(D)$ is the normalized distribution function of defect density (pdf).
- Three distributions of $D_0A$ are evaluated;

$$Delta\ function: Y_1 = e^{-D_0 A}$$

$$Triangular: Y_2 = \left\{ \frac{1 - e^{-D_0 A}}{D_0 A} \right\}^2$$

$$Rectangular: Y_3 = \frac{1 - e^{-2D_0 A}}{2D_0 A}$$

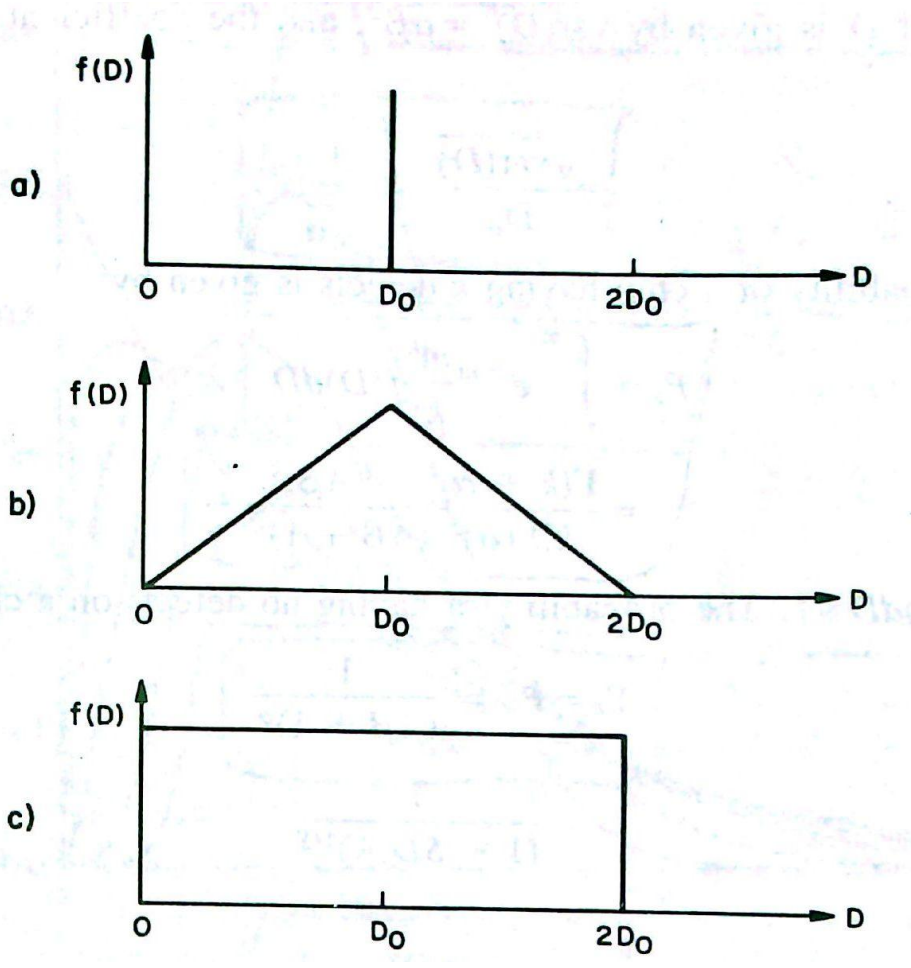



Fig: Distribution of density (a) Delta function (b) Triangular (c) Rectangular

# Contd...

- Consider $D_0A>>1$.

$$\lim_{D_0A>>1} Y_1 = e^{-D_0A}$$

$$\lim_{D_0A>>1} Y_2 = \left\{\frac{1}{D_0A}\right\}^2$$

$$\lim_{D_0A>>1} Y_3 = \frac{1}{2D_0A}$$

- Out of these three expressions, $Y_3$ gives yield of large ICs.

# 3. The Gamma Distribution of D

- In this case, probability density function is given by;

$$\left.\begin{aligned} f(D) &= \frac{1}{\Gamma(\alpha)\beta^{\alpha}} D^{\alpha-1} e^{-D/\beta} \\ D, \alpha, \beta &> 0 \end{aligned}\right\} \alpha, \beta \text{ are two distribution parameters and } \Gamma(\alpha) \text{ is Gamma function}$$

$$\text{where } \Gamma(\alpha) = (\alpha - 1)!$$

- In this distribution, the average density of defects is given by; $D_0 = \alpha\beta$
- The variance of D is given by; $\text{var}(D) = \alpha\beta^2$
- And the coefficient of variation is given by; $\frac{\sqrt{\text{var}(D)}}{D_0} = \frac{1}{\sqrt{\alpha}}$
- The probability of a chip with area A having k defects is given by

$$P_k = \int_0^{\infty} e^{-m} \frac{m^k}{k!} f(D) dD$$

$$= \frac{\Gamma(k+\alpha)}{k!\Gamma(\alpha)} \frac{(A\beta)^k}{(A\beta+1)^{k+\alpha}}$$

# Contd...

- The probability of having no defects on a chip is given by;

$$Y_4 = P_0 = \frac{1}{(A\beta + 1)^{\alpha}}$$

$$= \frac{1}{(1 + SD_0A)^{1/S}} \quad where\ S = \frac{\text{var}(D)}{D_0^2} = \frac{1}{\alpha}$$

- Figure on next slide, shows the shape of distribution function for several values of S.
- When S tends to zero, the Gamma distribution reduces to delta function.

$$f(\text{D}) = \delta(D - D_0)$$

- Where, $S \cong 0, \beta = SD_0$ and yield $Y_4$ is given by; $Y_4 = e^{-D_0A}, S \to 0$

Fig: Gamma Distribution of defect density

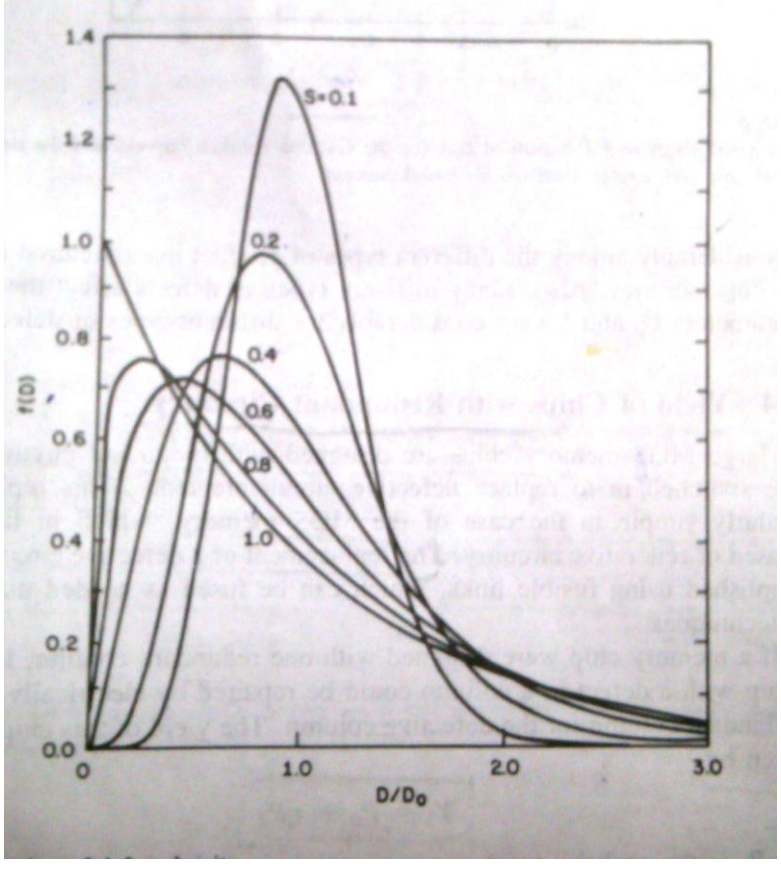
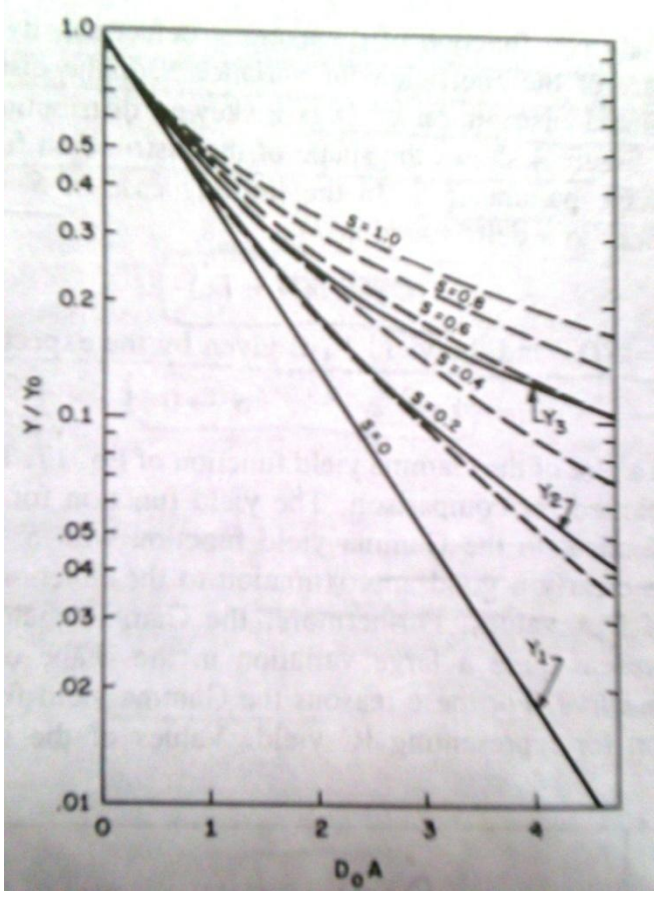



Figure: Yield of Good chips as a function of $D_0A$ for Gamma (broken curves) and the delta function, triangular, and rectangular distributions (solid curves)



# Contd...

- From the figures shown on previous slide; the yield function for uniform density of $D_0, Y_1$ is identical to GammaYield function with $S = 0$.
- The GammaYield function is the most common function for representing IC Yield, because it can represent a large variation in the shape parameter S.

# 4. Yield of Chips with Redundant Circuitry

- The MOS based memory circuits are designed with redundant circuitry.
- The defective circuits can be replaced by redundant circuits.
- These redundant circuits can be used as fusible links.
- These can be fused as per requirement.
- The yield of this kind of chip is given by; $Y_1 = P_0 + \eta P_1$
- Where $P_0$ is the probability of a chip containing no defect, $P_1$ is the probability of chip containing 1 defect, and $\eta$ is the probability of a chip containing 1 defect that can be repaired by using the single redundant column.

# 5. Multiple Types of Defects

- There are lot of defects on an IC. Each kind of defect affects different IC on the wafer.
- Example: defect in gate oxide affects gate oxide of the transistor.
- Junction leakage caused by oxidation induced staking faults affects both the gate and source/drain regions.
- The yield loss in VLSI depends upon different defect mechanisms.
- Each defect mechanism can be characterized by its mean defect density $D_{n0}$, the shape factor $S_n$, and the portion of the total chip area $A_n$.
- By GammaYield function, the yield for each type of defect is

$$Yn = \frac{1}{(1+S_n A_n D_{n0})^{1/S_n}}$$

# Contd...

- The overall yield is the product of the yield for each known type of defect;

$$Y = \prod_{n=1}^{N} Y_n = \prod_{n=1}^{N} \frac{1}{(1 + S_n A_n D_{n0})^{1/S_n}}$$

- The yield will be maximum when, $S_n A_n D_{n0} << 1$ . The Yield in this case will be,

$$\ln Y = \ln \prod_{n=1}^{N} Y_n = \sum_{n=1}^{N} \left[ -\frac{1}{S_n} \ln(1 + S_n A_n D_{n0}) \right] \approx \sum_{n=1}^{N} \left[ -\frac{1}{S_n} S_n A_n D_{n0} \right]$$

$$= \sum_{n=1}^{N} \left[ -A_n D_{n0} \right] \quad or \quad Y = \exp\left( -\sum_{n=1}^{N} \left[ A_n D_{n0} \right] \right) = e^{-A\overline{D}}$$

$$where, \overline{D} = \frac{1}{A} \sum_{n=1}^{N} \left[ A_n D_{n0} \right]$$

# Contd...

- In this equation the yield is represented by an exponential and independent of the shape parameter S for each type of defect.
- If there are M multiple chip sites then yield is given by;

$$Y_M = e^{-MA\overline{D}}$$

# 6. Radial Distribution of Defects

- If the defects of density varies as a function of the radius of the wafer, then the defects of density is given by;

$$D(r) = D_0 + D_R\, e^{(r-R)/L}$$

- Where
  - $D_0$ is the defect of density associated with the center of the wafer,
  - $D_R$ is the increase in defect of density at the edge of the wafer,
  - r is the radial coordinate,
  - R is the radius of the wafer,
  - L is the characteristic length associated with the edge related defects.

# Contd...

- The yield of the wafer with a radial distribution of defects may be obtained by integrating the poisson yield function over the area of the wafer;

$$Y_R = \frac{2}{R^2}\int_0^R e^{-D(\mathrm{r})\mathrm{A}}\,\mathrm{rdr}$$

- The yield can be calculated for delta function or Gamma function as discussed in previous cases.

# Reliability requirements for VLSI

- Lot of defects and their yield has been discussed already.
- If we take one device failure out of 10000 devices per month as a goal, then the devices must have a failure rate, $\lambda$ of

$$\lambda < \frac{1 Failure}{10^5 \; Devices \; X \; 720 \; Hours}$$

$$= 14 \; X \; 10^{-9} \; Failure / Devices - hour$$

- The failure Unit = 1 FIT = 1 failure/$10^9$ Devices-hour.
- Then as per our case, the device failure rate is $\lambda < 14$ FIT.
- Over the 10 years life of the system, 120 devices will be failed.
- Effect of failure is summarized in the tables.

| | Effect of transistor failure on system performance (1,00,000 devices) | | Effect of device failure on modern system performance (150 to 225 ICs) | | Private Telephone system (10,000 ICs) | |
|---|---|---|---|---|---|---|
| Failure Rate (FIT) | Failure/Month | Total % of devices to fail in 10 years | Man Time to data Set Failure (Years) | % of Sets fail/month | System failure/month | % of circuit packs fail in 10 Years |
| 10 | 0.7 | 0.1 | 51 | 0.16 | 0.07 | 1 |
| 100 | 7 | 1 | 5 | 1.6 | 0.7 | 10 |
| 1000 | 70 | 10 | 0.5 | 16 | 7 | 65 |

# Accelerated Testing

- The failure rate of an IC must be on the order of 100 FIT or less.
- Under normal operating conditions, with a failure rate of 100 FIT, the time required to observe one failure in 100 devices is about 1,00,000 hours (11.4 years).
- We must find the methods to accelerate the mechanisms that cause devices to failure.
- There are five common stresses used to accelerate device failure mechanisms;
  a. Temperature
  b. voltage
  c. Current
  d. Humidity
  e. Temperature cycle

# Contd...

- A device may fail at normal operating conditions because of two completely different failure mechanisms.
- Accelerating testing is a useful tool, if we know the device failure mechanisms.

# A. Temperature Acceleration

- Chemical and physical processes can cause a failure in a device.
- These processes can be accalerated by temperature in order to reduce failure.
- The reaction rate R, at which these processes are governed is given by Arrhenius equation;

$$R = R_0 \exp(-E_a/kT)$$

- Where
  - $E_a$ is the activation energy (eV) of the process
  - k is Boltzmann constant ($8.6 \times 10^{-5}$ eV/K)
  - T is the temperature (K)

# Contd...

- Some parameter of the IC changes as a function of time.
- These parameter has some initial value.
- The IC failure takes place when the parameter exceeds some value.
- Figure shows the parameter increasing at different rates at two temperatures $T_1$ and $T_2$ ($T_2 > T_1$).
- The failure takes place at time $t_1$ and $t_2$ respectively ($t_1 > t_2$).
- Using Arrhenius equation; the ratio of two times to failure is given by;

$$\frac{t_1}{t_2} = \frac{R_2}{R_1} = \exp\left[\frac{E_a}{k}\left(\frac{1}{T_1} - \frac{1}{T_2}\right)\right]$$

- This equation is **acceleration factor** due to the increased temperature.

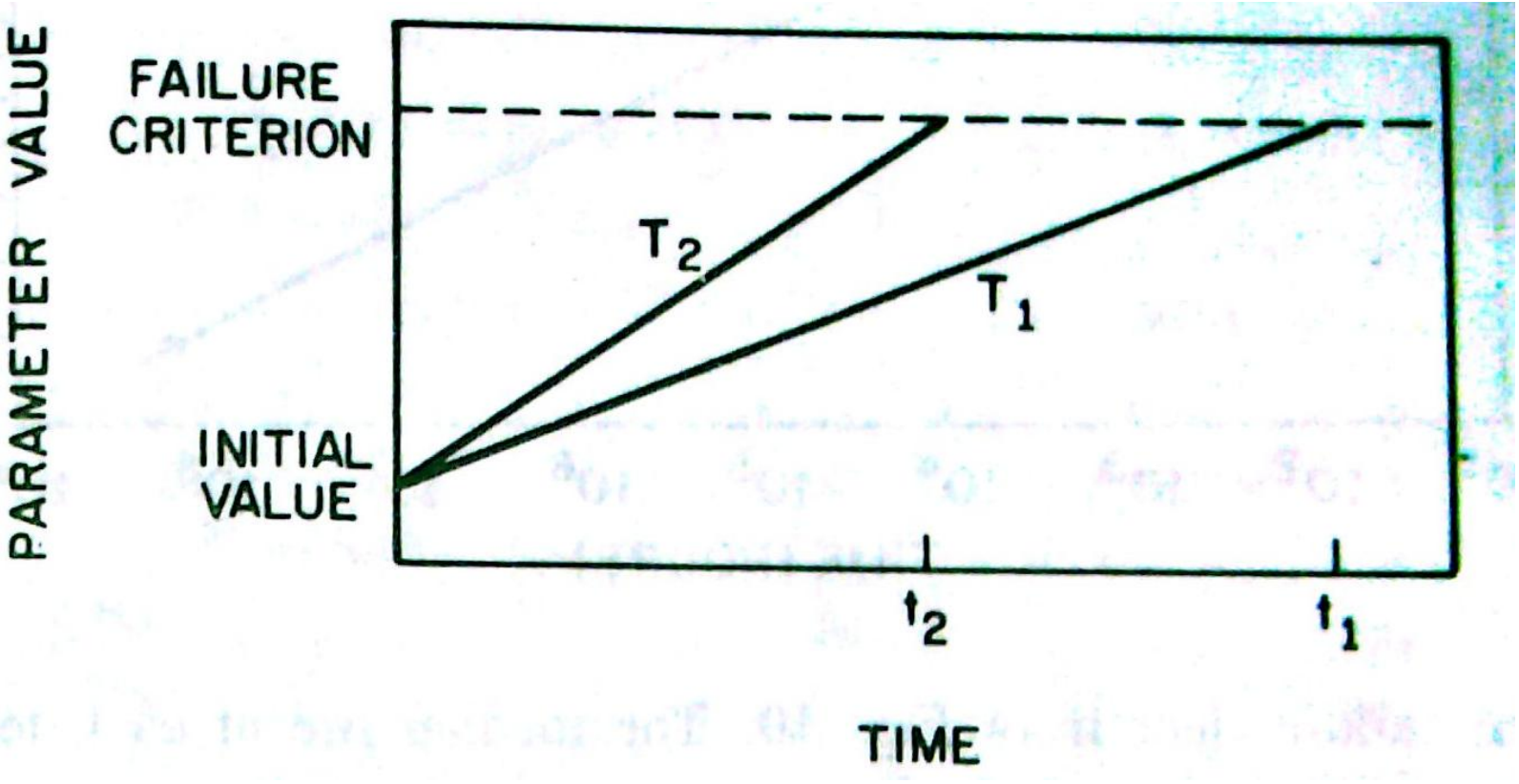



Figure: Change of parameter value with time at different temperatures

# Contd...

- IC failure occurs when the destructive (much damage) reaction has proceeded to some value equal to the failure criterion.
- It means the product of the reaction rate R and the time to failure $t_F$ is a constant.
- The time to failure at different temperatures is given by;

$$t_F = \frac{constant}{R} = constant\ x \exp(E_a / kT)$$

or

$$\ln t_F = constant + E_a / kT$$

- Figure on next slide shows a plot of the median time to failure at three different temperatures (175, 200, 250 $^{O}$C) versus inverse absolute temperature.

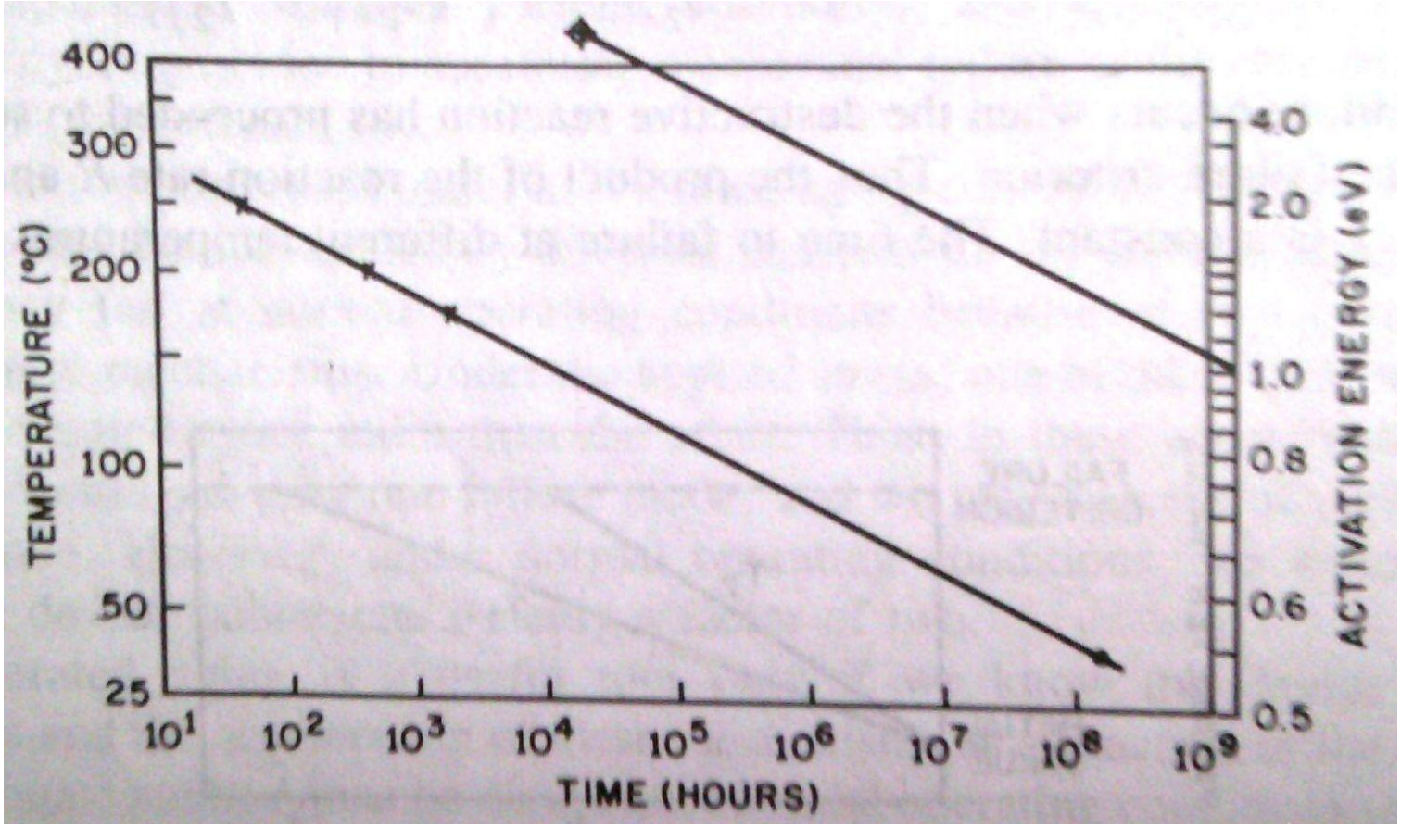



Figure: Arrhenius Plot of the failure

# Contd...

- The median life at a temperature of 40 $^{0}$C is approximately 2 X $10^{8}$ hours.
- Table on next slide summarizes the acceleration factor due to operating at an increased temperature for two values of the activation energy.
- For a failure mechanism with a 1.0 eV activation energy, 11 hours of operation at 200 $^{O}$C is equivalent to 40 years of operation at 60 $^{O}$C.
- In above discussion, we assumed that the activation energy is positive, that is, that devices fail faster at higher temperatures.
- The hot electrons generated in the silicon are captured in the gate oxide, causing a shift with time in the threshold voltage.
- The captured electrons are gradually released back to the silicon; the higher the temperature, the greater the release rate.

# Table: Acceleration factor and time equivalent to 40 years

| $T_{high}$ ($^{O}C$) | Acceleration factor | | Time (h) equivalent to 40 years | |
|---|---|---|---|---|
| | Ea = 1.0 eV | 0.5 eV | 1.0 eV | 0.5 eV |
| 300 | $2.2 X10^{6}$ | 1500 | 0.2 | 233 |
| 250 | $3.2 X 10^{5}$ | 570 | 1.1 | 616 |
| 200 | $3.1 X 10^{4}$ | 176 | 11 | 2000 |
| 150 | 1700 | 41 | 200 | 8526 |
| 125 | 300 | 17 | 1200 | 20,200 |
| 85 | 11.5 | 3.4 | 30,000 | 103,000 |

# Contd...

- At higher temperature, no shift is seen in threshold voltage, because the release rate is equal to or greator than the capture rate.
- At low temperatures very large shifts in threshold voltage are seen, because the release rate becomes much smaller than the capture rate.

# B. Voltage and Current Acceleration

- Voltage and current are effective accelerating stresses for many of the common failure mechanisms observed in ICs.
- Voltage ( in some cases electric field) causes acceleration of failure caused by dielectric breakdown, interface charge accumulation, charge injection etc.
- With most of the ICs, varying the applied voltage over a very large range is not possible.
- A device designed to operate at 5 V usually will not function properly if the applied voltage is outside the 4 to 7 V range.
- The reaction rate R of the failure mechanism is proportional to a power of applied voltage;

$$R(T,V) = R_0(T)V^{\gamma(T)}$$

# Contd...

- The coefficient $R_0(T)$ is an Arrhenius function of T, and parameter $\gamma(T)$ varies between 1 to 4.5.
- thus, if we operate a given device at 7 V rather than 5 V we can accelerate the failure.
- In the case of dielectric breakdown, a different type of acceleration occurs.
- he reaction rate of the electromigration is a function of temperature and current density.

$$R(T,J) = R_0(T)J^{\gamma(T)}$$

- In this case parameter $\gamma(T)$ varies form 1 to 4.
- IC testing is done in order to determine the maximum allowable current density for which the failure rate of conductors will be acceptable.

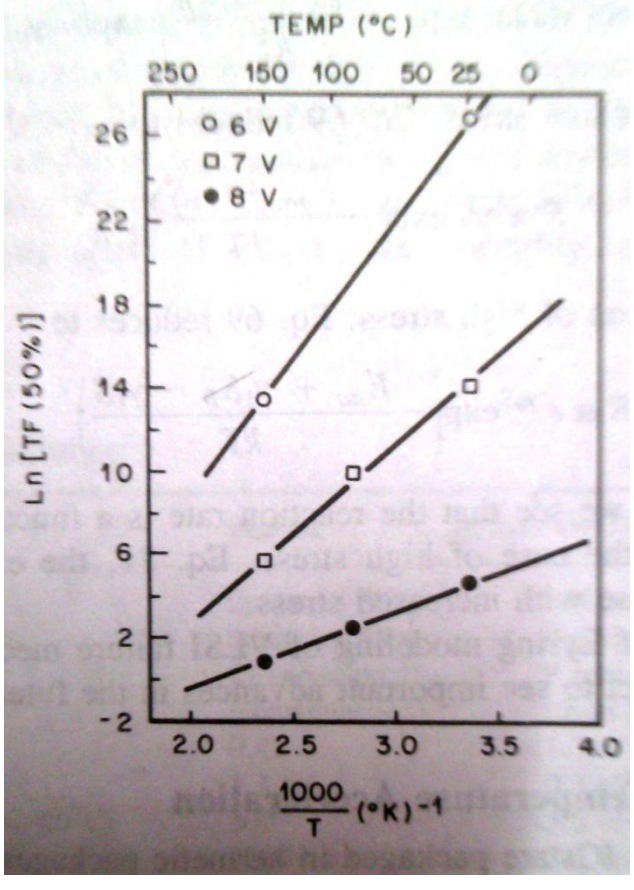
# C. Stress Dependent Activation Energy

- The activation energy to cause failures accelerated by voltage (dielectric breakdown) and current (electromigration) depends upon the applied stress (See Next Slide).
- Thermally and stress activated failure mechanisms as given by Eyring model.
- The Eyring model assumes that the energy required for reaction to take place is affected by the applied stress (voltage and current).
- The reaction rate of the failure mechanism, R is given by;

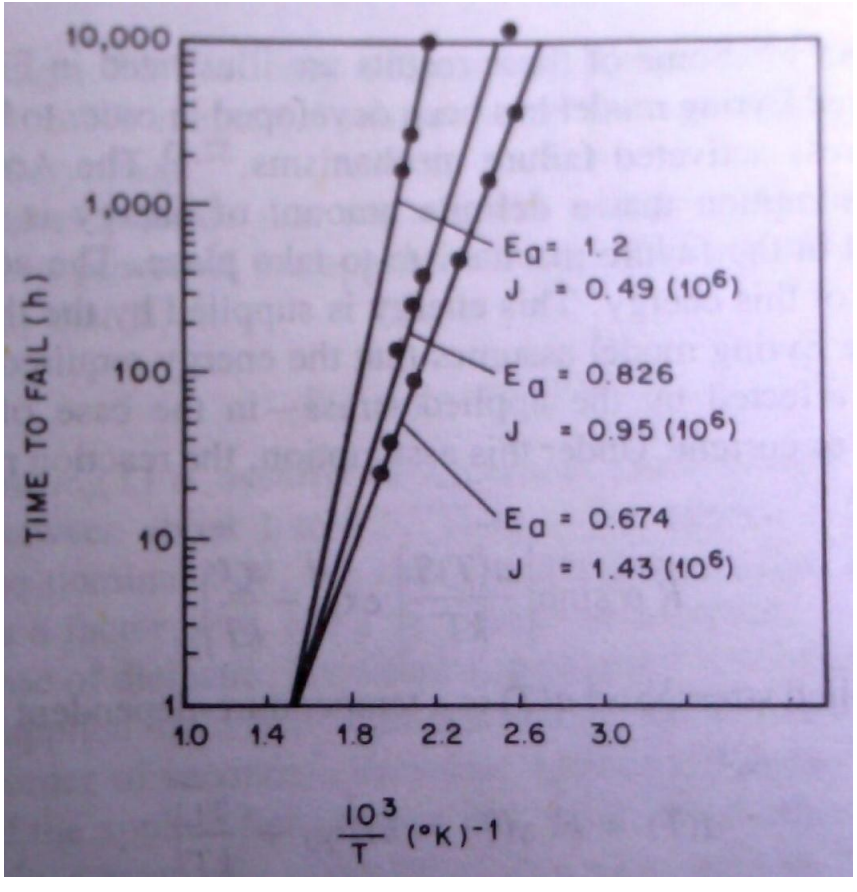
$$R \alpha \sinh\left[\frac{a(\mathrm{T})\mathrm{S}}{kT}\right]\exp\left(-\frac{Q}{kT}\right)$$

- Where
  - S is applied stress,
  - *a(t)* is a temperature dependent parameter.

## Figure: Arrhenius Plot of Time to Failure data for $SiO_2$ dielectric breakdown.




## Figure: Arrhenius Plot of Time to Failure data for electromigration in Al-Si metallization



# Contd...

$$a(\mathrm{T}) = \mathrm{kT}\,\gamma(\mathrm{T}) = \mathrm{kT}\left(\gamma_0 + \frac{\gamma_1}{kT}\right)$$

- Q is related to the Arrhenius activation energy and is given by;

$$Q = E_{a0} + a(\mathrm{T})\mathrm{S_B}$$

- Where $S_B$ is the breakdown stress, the value of applied stress where of the device occurs essentially instantaneously.
- The reaction rate can also be expressed as;

$$R\alpha \sinh\left[\gamma(\mathrm{T})\mathrm{S}\right]\exp\left(-\frac{E_{a0} + \gamma_1 S_B}{kT}\right)\exp\left(-\gamma_0 S_B\right)$$

- The above equation under low stress conditions reduces to;

$$R\alpha\,\gamma\,\mathrm{S}\exp\left(-\frac{E_{a0} + \gamma_1 S_B}{kT}\right)$$

# Contd...

- While under the high stress conditions;

$$R \alpha e^{\gamma_0 S} \exp\left(-\frac{E_{a0} + \gamma_1 S_B - \gamma_1 S}{kT}\right)$$

- From above equations, we can see that the reaction rate is a function of the applied stress $S$.
- The activation energy decreases with increased stress.

# D. Humidity-Temperature Acceleration

- The water vapor present in the chip may cause failure mechanisms.
- The water vapor quickly penetrates plastic material.
- The water vapor transports contaminations from the surface of the package through the plastic.
- After that water vapor leaches (extraction of certain materials into a liquid) impurities from the plastic packaging material itself.
- The surface of the chip is very quickly exposed to the water vapor and various contaminations.
- The second step is the diffusion of the contaminated water vapor through the passivation layer of the chip.

# Contd...

- If the passivation layer contains defects or cracks, the water vapor penetrates through the wafer more quickly.
- Once the water vapor reaches the metallization level of the chip, electrochemical corrosion (degradation of a material due to a reaction) can occur.
- The ions needed for corrosion process can arise from two sources.
- Ions can diffuse as a contaminant through the passivation layer along with the water vapor.
- If the intermediate dielectric of the chip is a phosphorus doped glass, the water vapor can leach phosphorus from the intermediate dielectric.
- If the electrochemical corrosion is very rapid, metallization failure occurs.

# Contd...

- This type of failure mechanism can be accelerated by increasing the partial pressure of water vapor in the environment.
- Table summarizes the analysis for the acceleration of the failures for BJT and NMOS.
- For each device, and each failure mechanism in that device, the accelerating effect of temperature, humidity, and voltage must be redetermined.

# Table: Humidity-induced failures

| Device | BJT | NMOS |
|---|---|---|
| Passivation Layer | Sputtered $SiO_2$ | SiN |
| Intermediate Dielectric | Sputtered $SiO_2$ | P Glass |
| Mechanism | Cl Corrosion (Contamination) | P Corrosion (from P Glass) |
| $\sigma$ | 0.43 | 1.34 |
| $E_a$ | 1.1 eV | 0.3 eV |
| Accelerating Factor | 300 | 5.5 |
| 40Yr/Acceleration | 1200 Hours | 7.3Years |

# E. Burn - in

- Oxide pinholes, photoresist or etching defects, contamination on the chip or in the package, weak chip or wire bonds and partially chips or packages are the most common failure factors.
  If the steady state failure rate is extremely low, then this kind of failure rate known as infant mortality (deadly) failure & is easily modeled using Weibull model.
- For this case the overall failure rate is expressed as;

$$\lambda(t) = \frac{\beta}{\alpha} t^{\beta-1} + \lambda_{SS}$$

- Where $\lambda(t)$ is the device failure rate, $\beta$ and $\alpha$ are the parameters of the infant mortality failure distribution and $\lambda_{SS}$ is the constant steady state failure rate.
- In burn-in procedure, the devices are operated for some period of time, during the infant mortality failure.

# Contd...

- The burn-in consist of operating the device under conditions of increased temperature, increased voltage, and high current.
- If devices are operated under burn-in conditions for some time, $t_{BI}$, where the acceleration of the infant mortality failures is $A_{BI}$, then the failure rate of the device is given by;

$$\lambda_{EFF}(t) = \lambda(t+t_0) = \lambda(t + t_{BI} \, . A_{BI})$$

- The infant mortality failures can also eliminate by eliminating weak chips or wire bonds and partially cracked chips or packages.

# Review Questions

- Why packaging is required? Explain flip chip technology. **[UTU 2012]**
- Write short note on package types and packaging design VLSI Technology. What is meant by DIP? Explain in brief. **[UTU 2011]**
- Write a short note on VLSI assembly technologies. Describe the different VLSI assembly technologies. **[UTU 2011]**
- How is packaging evaluated for VLSI design? Discuss the types of packaging design consideration. **[UTU 2013]**
- Write a detailed note on different yield loss mechanisms in VLSI. **[UTU 2011]**

# Contd...

- Explain why modeling of yield loss mechanisms is required. Explain general model of yield loss mechanism and also explain accelerated testing in brief. **[UTU 2012], [UTU 2013]**
- What do you mean by Yield in VLSI? How you can have the products with overall high Yield? Explain the trade-offs also to achieve the high yield. **[UTU 2012]**
- Explain the reliability in terms of VLSI technology. Explain how is accelerated testing performed? **[UTU 2013]**