UNIT III – IC 741 OP-AMP
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The 741 OPAMP Circuit: Bias circuit, short circuit protection, the input stage, the second stage, the output stage, the Device parameters

DC Analysis of 741: Reference bias current, input stage bias, input bias and offset current, input offset voltage, input common range, second stage bias, output stage bias

Small Signal Analysis of 741: The input stage, second stage, the output stage

Gain, Frequency Response and Slew rate of 741: Small signal gain, frequency response, a simplified model, slew rate, relationship between $F_t$ and SR
Basics of IC 741
Manufacturers of IC 741

- It is possible to identify the manufacturer by looking at the number printed on the OP-AMP IC. Fairchild first produced it and sold it as “μA741” where “μA” represent the initials for Fairchild and 741 as OP-AMP.
- Fairchild: μA741
- National semiconductor: LM741
- Motorola: MC1741
- RCA: CA3741
- Texas instrument: SN52741
- Signetics: N5741
PIN CONFIGURATION

offset null 1 8 n/c
inv. input 2 7 V+
non-inv. input 3 6 output
V- 4 5 offset null

8-Pin
OP-AMP IC 741 - DESCRIPTION

- This IC is an 8 pin IC in the dual in line (DIP) package.
- This is one of the oldest and one of the most popular Op-amp IC.
- It is a high performance monolithic operational amplifier.
- It has wide range of applications such as integrator, differentiator, summing amplifier etc.
**DEFINITION OF 741-PIN FUNCTIONS**

- **Pin 1 (Offset Null):** Offset voltage is nulled by application of a voltage of opposite polarity to the offset.
- **Pin 2 (Inverted Input):** All input signals at this pin will be inverted at output pin 6.
- **Pin 3 (Non-Inverted Input):** All input signals at this pin will be processed normally without inversion.
- **Pin 4 (-V):** The V- pin (also referred to as \( V_{cc} \)) is the negative supply voltage terminal.
- **Pin 5 (Offset Null):** Same pin 1.
- **Pin 6 (Output):** Output signal's polarity will be the opposite of the input's when this signal is applied to the op-amp's inverting input.

- **Pin 7 (+V):** The V+ pin (also referred to as $V_{cc}$) is the positive supply voltage terminal of the 741 Op-Amp IC.

- **Pin 8 (N/C):** The 'N/C' stands for 'Not Connected'. There is no other explanation. There is nothing connected to this pin, it is just there to make it a standard 8-pin package.
ABSOLUTE MAXIMUM RATINGS

- **Supply voltage**: ±18V
- **Internal power dissipation**
  - Metal package: 500 mW
  - DIP: 510 mW
  - Flat pack: 570 mW
- **Storage temperature range**
  - Metal package: -65°C to +150°C
  - DIP: -55°C to +125°C
- **Operating temp range**
  - Military: -55°C to +125°C
  - Commercial: 0°C to +70°C
## Important Characteristics of IC 741

<table>
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<th>Sr. No.</th>
<th>Characteristics</th>
<th>Value for IC 741</th>
<th>Ideal Value</th>
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<tr>
<td>1.</td>
<td>Input Resistance</td>
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<td>Output Resistance</td>
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<td>5.</td>
<td>Slew Rate</td>
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</table>
THE 741 OP-AMP CIRCUIT

Bias Circuit, Short Circuit Protection, The Input Stage, The Second Stage, The Output Stage, The Device Parameters
Figure 1: The 741 op-amp circuit. $Q_{11}$, $Q_{12}$, and $R_5$ generate a reference bias current, $I_{\text{REF}}$. $Q_{10}$, $Q_9$, and $Q_8$ bias the input stage, which is composed of $Q_1$ to $Q_7$. The second gain stage is composed of $Q_{16}$ and $Q_{17}$ with $Q_{13B}$ acting as active load. The class AB output stage is formed by $Q_{14}$ and $Q_{20}$ with biasing devices $Q_{13A}$, $Q_{18}$, and $Q_{19}$, and an input buffer $Q_{23}$. Transistors $Q_{15}$, $Q_{21}$, $Q_{24}$, and $Q_{22}$ serve to protect the amplifier against output short circuits and are normally cut off.
Initially IC 741 was manufactured by “Fairchild Corporation”.

It consists of 24 transistors, 11 resistors and 1 capacitor.

IC 741 requires two power supplies, $+V_{CC}$ and $-V_{EE}$.

Normally $+V_{CC} = +15 \text{ V}$ and $-V_{EE} = -15\text{ V}$.

The IC 741 is capable of operating at much lower power supply voltages (upto $\pm 5\text{ V}$).
BIAS CIRCUIT
The reference bias current of the 741 circuit, \( I_{\text{REF}} \), is generated in the branch at the extreme left of Fig. 1, \( Q_{11} \) and \( Q_{12} \) and the resistance \( R_5 \).
Widlar current source is formed by $Q_{11}$ and $Q_{10}$ and the resistance $R_4$.

The bias current for the first stage is generated in the collector of $Q_{10}$. 

$\begin{align*}
I_{REF} & \quad Q_{11} \\
& \quad R_4
\end{align*}$
There is another current mirror formed by $Q_8$ and $Q_9$ which is responsible for the biasing in the first stage.
• $Q_{13}$ is double-collector lateral $pnp$ transistor.
• The transistors $Q_{12}$ and $Q_{13}$ form a two-output current mirror.
• Collector of $Q_{13A}$ provides the bias current for the output stage of the op amp.
• The purpose of $Q_{18}$ and $Q_{19}$ is to establish the two $V_{BE}$ drops between the bases of the output transistors $Q_{14}$ and $Q_{20}$. 
SHORT-CIRCUIT PROTECTION CIRCUITRY
The 741 circuit includes large number of transistors that are normally off and conduct only when large output current is required.

The large current can be achieved at the output terminals if the output terminal is short-circuited to one of the two supplies.

This circuit protects the IC if an excess load current is drawn from it.

The short-circuit protection network consists of \( R_6, R_7, Q_{15}, Q_{21}, Q_{24}, R_{11} \) and \( Q_{22} \).
Input stage consists of transistors through $Q_1$ to $Q_7$.
The biasing is performed by transistors $Q_8$, $Q_9$ and $Q_{10}$.
Transistors $Q_5$, $Q_6$ and $Q_7$ and resistors $R_1$, $R_2$ and $R_3$ form the load circuit of the input stage.
Every OP-AMP circuit uses a level shifter.
The function of level shifter is to shift the dc level of the signal so that the signal at the OP-AMP output can swing positive and negative.
In 741, level shifting is done in the first stage using the lateral pnp transistors $Q_3$ and $Q_4$. 
THE SECOND STAGE
The second stage or intermediate stage is composed of $Q_{16}$, $Q_{17}$, $Q_{13B}$, and two resistors $R_8$ and $R_9$.

- Transistor $Q_{16}$ acts as an emitter follower.
- So it provides high input resistance to the second stage.
- This minimizes the loading on the input stage and avoids the loss of gain.
- Transistor $Q_{17}$ acts as an common-emitter amplifier with a 100 Ω resistance in its emitter.
Its load is composed of the high output resistance of the \textit{pnp} current source $Q_{13B}$ in parallel with the input resistance with the output stage.

The output of the second stage is taken at the collector of $Q_{17}$.

Capacitor $C_C$ is connected in the feedback path of the second stage to provide frequency compensation.

Capacitor $C_C$ is small in value.

The chip are for Capacitor $C_C$ is about 13 times that of a standard \textit{npn} transistor.
THE OUTPUT STAGE
741 uses class AB output stage.
The purpose of the output stage is to provide the amplifier with low output resistance.
Emitter follower circuit is the class A output stage.
The drawback of the class A output stage is large power dissipated in the transistor.
This power dissipation can be reduced by arranging the transistor to turn on only when an input signal is applied.
Figure 2 (a) The emitter follower is a class A output stage. (b) Class B output stage (c) The output of a class B output stage fed with an input sinusoid. Observe the crossover distortion. (d) Class AB output stage.
So in order to reduce the power dissipation two transistors are required.

An npn to source the output current and a pnp transistor to sink the output current.

This kind of arrangement is called class B output stage.

Both the transistors will be cutoff when $v_I = 0$.

When $v_I$ goes positive $Q_N$ conducts while $Q_P$ remains off.

When $v_I$ goes negative transistors reverse roles.

Class B output stage is efficient in power dissipation, but the output signal is distorted.
Output signal is distorted when $|v_I|$ is less than about 0.5, neither of the transistors will conduct.

This is called crossover distortion.

Crossover distortion can be reduced by biasing the output stage transistors at low current.

In this case, the output stage transistors will remain conducting when $v_I$ is small.
THE DEVICE PARAMETERS
For the standard \( npn \) and \( pnp \) transistors, the following parameters will be used:

- \( npn \): \( I_s = 10^{-14} \text{A}, \beta = 200, V_A = 125 \text{V} \)
- \( pnp \): \( I_s = 10^{-14} \text{A}, \beta = 50, V_A = 50 \text{V} \)

In 741 circuit the nonstandard devices are \( Q_{13}, Q_{14} \) and \( Q_{20} \).

For transistor \( Q_{13} \),

- \( I_{SA} = 0.25 \times 10^{-14} \text{A} \quad I_{SB} = 0.75 \times 10^{-14} \text{A} \),

Transistors \( Q_{14} \) and \( Q_{20} \) have an area three \textit{time} that of a standard device.
EXERCISE

For the circuit shown Fig, neglect base currents and use the exponential $i_c - v_{BE}$ relationship to show that

$$I_3 = I_1 \sqrt{\frac{I_{S3} I_{S4}}{I_{S1} I_{S2}}}$$
DC Analysis of 741

Reference bias current, input stage bias, input bias and offset current, input offset voltage, input common range, second stage bias, output stage bias
For the dc analysis of an op-amp circuit, the input terminals are grounded.

This should result in zero dc voltage at the output.

However, because the op amp has very large gain, the output voltage is close to either $+V_{CC}$ or $-V_{EE}$.

To overcome this problem in the dc analysis, it will be assumed that the op amp is connected in a negative feedback loop that stabilizes the output dc voltage to zero volts.
REFERENCE BIAS CURRENT
The reference Bias current $I_{REF}$ can be obtained as:

$$I_{REF} = \frac{V_{CC} - V_{EB12} - V_{BE11} - (-V_{EE})}{R_5}$$

For $V_{CC} = V_{EE} = 15 \text{ V}$ and $V_{BE12} = V_{EB12} = 0.7 \text{ V}$, we have $I_{REF} = 0.73 \text{ mA}$. 
Input-Stage Bias
Transistor $Q_{11}$ is biased by $I_{\text{REF}}$, and the voltage developed across it is used to bias $Q_{10}$ which has a series emitter resistance $R_4$.

**Figure** The Widlar current source that biases the input stage
From the circuit, and assuming $\beta_{10}$ to be large, we have,

$$V_{BE11} - V_{BE10} = I_{C10} R_4$$

Now assume that, $I_{S11} = I_{S10}$ we get,

$$V_T \ln \frac{I_{REF}}{I_{C10}} = I_{C10} R_4$$

At room temperature $V_T = 25$ mV.

For our case $I_{C10} = 19$ µA.
EXERCISE

- Design the Widlar current source to generate a current \( I_{C10} = 10\mu A \) given that \( I_{REF} = 1mA \). If at a collector current of 1mA, \( V_{BE} = 0.7 \) V, find \( V_{BE11} \) & \( V_{BE10} \).
Now we can determine dc current in each of the input-stage transistors.

**Figure:** The dc analysis of the 741 input stage.
From the Fig shown on previous slide, from symmetry we see that,
- \( I_{C1} = I_{C2} = I \)

If \( \beta_p \) is high, then for transistors \( Q_3 \) & \( Q_4 \),
- \( I_{E3} = I_{E4} = I \)

And base currents of \( Q_3 \) & \( Q_4 \) are equal, i.e.,
- \( I_{B3} = I_{B4} = I/\beta_p \).

Now consider current mirror formed by \( Q_8 \) & \( Q_9 \), at node X, if \( \beta_p \) is very larger than 1,
- \( I_{C10} = 2I \)

For the 741 circuit, \( I_{C10} = 19 \, \mu\text{A} \). So, we can determine that,
- \( I_{C1} = I_{C3} = I_{C3} = I_{C4} = 9.5 \, \mu\text{A} \)
Now consider the remainder circuit of the 741 input stage,

This part of the circuit is fed by \( I_{C3} = I_{C4} = I \)

Transistors \( Q_5 \) & \( Q_6 \) are identical so, \( I_{C3} = I_{C4} = I \)

The bias current of the \( Q_7 \) is given by,

\[
I_{C7} = I_{E7} = \frac{2I}{\beta_N} + \frac{V_{BE6} + IR_2}{R_3}
\]

The vale of \( V_{BE6} \) can be determined as,

\[
V_{BE6} = V_T \ln \frac{I}{I_s}
\]

Now substituting \( I_s = 10^{-14}A, \ I = 9.5 \ \mu A \), gives,
\( V_{BE6} = 517 \ \text{mV} \) & \( I_{C7} = 10.5 \ \mu A \).
Input Bias and Offset Currents
The input bias current of an op amp is defined as

\[ I_B = \frac{I_{B1} + I_{B2}}{2} \]

For the 741 we obtain \( I_B = \frac{I}{\beta_N} = 47.5 \text{nA} \)

Because of possible mismatches in the \( \beta \) values of \( Q_1 \) and \( Q_2 \) the input base currents will not be equal.

In this case, **input offset current** is defined as,

\[ I_B = |I_{B1} - I_{B2}| \]
Input Offset Voltage
Input offset voltage is the differential voltage that exists between two input terminals of an op-amp, without any external inputs applied.

In other words, it is the amount of the input voltage that should be applied between two input terminals in order to force the output voltage to zero.

In the 741 circuit, Input offset voltage is due to mismatch between $Q_1$ and $Q_2$, between $Q_3$ and $Q_4$, between $Q_5$ and $Q_6$ and between $R_1$ and $R_2$. 
INPUT COMMON MODE RANGE

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The input common-mode range is the range of Input common-mode voltages over which the input stage remains in the linear active mode.

For 741 circuit the input common-mode range is determined at the upper end by saturation of $Q_1$ and $Q_2$ and at the lower end by saturation of $Q_3$ and $Q_4$. 
SECOND STAGE BIAS
If we neglect the base current of $Q_{23}$, then we see that the collector current of $Q_{17}$ is approximately equal to the current supplied by current source $Q_{13B}$.

Because $Q_{13B}$ has a scale current 0.75 times that of $Q_{12}$.

Its collector current will be $I_{C13B} \approx 0.75I_{REF}$, where we have assumed that $\beta_P >> 1$.

Thus $I_{C13B} = 550\mu A$ & $I_{C17} \approx 550\mu A$.

Base-emitter voltage of $Q_{17}$ is

$$V_{BE17} = V_T \ln \frac{I_{C17}}{I_S} = 618mV$$
The collector current of $Q_{16}$ is given as,

$$I_{C16} \approx I_{E16} = I_{B17} + \frac{I_{E17} \cdot R_8 + V_{BE17}}{R_9}$$

Which gives, $I_{C16} = 16.2 \mu A$
OUTPUT-STAGE BIAS
Figure The 741 output stage without the short-circuit protection devices.
Current source $Q_{13A}$ delivers a current of $0.25I_{REF}$ (because $I_S$ of $Q_{13A}$ is 0.25 times the $I_S$ of $Q_{12}$).

Neglecting base currents of $Q_{14}$ & $Q_{20}$,
- $I_{C23} \approx I_{E23} \approx 0.25I_{REF} = 180 \, \mu A$.

If we assume that $V_{BE18}$ is approximately 0.6 V. we can determine the current in $R_{10}$ as 15 $\mu A$.

The emitter current of $Q_{18}$ is therefore
- $I_{E18} \approx I_{C18} = 180 - 15 = 165 \, \mu A$ & $V_{BE18} = 588 \, mV$.

The base current $I_{B18} = 165/200 = 0.8 \, \mu A$. So
- $I_{C19} \approx I_{E19} = 15.8 \, \mu A$

$V_{BE19}$ is determined as
\[
V_{BE19} = V_T \ln \frac{I_{C19}}{I_S} = 530 mV
\]
As, we know that the purpose of the transistors $Q_{18} - Q_{19}$ network is to provide two $V_{BE}$ drops between the bases of the output transistors $Q_{14}$ & $Q_{20}$.

This voltage drop $V_{BB}$ is given by,

- $V_{BB} = V_{BE18} + V_{BE19} = 588 + 530 = 1.118V$

Where

$$V_{BB} = V_T \ln \frac{I_{C14}}{I_{S14}} + V_T \ln \frac{I_{C20}}{I_{S20}}$$

Now putting values of $V_{BB}$, and $I_{S14} = I_{S20} = 3 \times 10^{-14}$ A, we get, $I_{C14} = I_{C20} = 154 \ \mu A$.

This is the small current at which class AB output stage is biased.
### SUMMARY

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<tr>
<th>Q_1</th>
<th>Q_2</th>
<th>Q_3</th>
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**Table 12.1** DC Collector Currents of the 741 Circuit (µA)
SMALL SIGNAL ANALYSIS OF 741

The input stage, second stage, the output stage
THE INPUT STAGE
Figure Small-signal analysis of the 741 input stage.
The differential signal $v_I$ applied between the input terminals.

The four transistors shown in figure are connected in series.

Emitter signal currents flow as indicated in Fig.

\[ i_e = \frac{v_I}{4r_e} \]

Where $r_e$ is emitter resistance of the four transistors shown in figure. Where,

\[ r_e = \frac{V_T}{I} = \frac{25\, \text{mV}}{9.5\, \mu\text{A}} = 2.63\, \text{k}\Omega \]

Input differential resistance is given by,

\[ R_{id} = 4(\beta_N + 1)r_e = 2.11\, \text{M}\Omega \]
Figure The load circuit of the input stage fed by the two complementary current signals generated by $Q_1$ through $Q_4$ in Fig. shown on previous slide. Circled numbers indicate the order of the analysis steps.
Assuming the base current of $Q_7$ to be equal to zero, so the collector current of $Q_5$ will be,

$$I_{c5} = \alpha i_e$$

Transistors $Q_5$ and $Q_6$ are identical and have identical emitter resistances, therefore,

$$I_{c6} = I_{c5} = \alpha i_e$$

So the load circuit behaves like a current mirror.

Consider output node of the input stage, the output current is given by,

$$i_0 = \alpha i_e + I_{c6} = \alpha i_e + \alpha i_e = 2\alpha i_e$$

Transconductance of the input stage is given by,

$$G_{m1} = \frac{i_0}{v_i} = \frac{2\alpha i_e}{4i_e r_e} = \frac{\alpha}{2r_e} = \frac{1}{2(2.63\ k\Omega)} = 1.9 \times 10^{-4} \ A/V$$
Figure Simplified circuits for finding the two components of the output resistance $R_{o1}$ of the first stage.
- Output resistance \((R_{01})\) of the input stage is the resistance seen looking back onto the collector of transistor \(Q_6\).
- From the figure shown on slide 64, we can say that, \(R_{01}\) is equal to the parallel combination of the output resistance of the current source \(ai_e\) and the output resistance of \(Q_6\).
- Assume that the base of \(Q_4\) is virtual ground.
- The \(R_{04}\) is given by, \(R_{04} = r_o[1 + g_m(r_e || r_\pi)]\)
- So, for \(Q_4\), \(r_e = 2.63 \text{ k}\Omega\), \(r_o = V_A/I\), \(V_A = 50\text{V}\), \(I = 9.5 \mu\text{A}\), \(r_\pi = (\beta+1)r_e >> r_e\), so neglecting it.
- So, \(R_{04} = 10.5 \text{ M}\Omega\).
The $R_{04}$ is given by, $R_{06} = r_o[1 + g_m(R_2 || r_\pi)]$

- So, for $Q_4$, $r_e = 2.63 \, \text{k}\Omega$, $r_o = V_A/I$, $V_A = 50V$, $I = 9.5 \, \mu\text{A}$,
  $r_\pi = (\beta+1)r_e >> r_e$, so neglect it.
- So, $R_{06} = 18.2 \, \text{M}\Omega$.

Hence, the output resistance of the input stage is given by, $R_{01} = 6.7 \, \text{M}\Omega$.

**Figure** Small-signal equivalent circuit for the input stage of the 741 op amp.
SECOND STAGE
**Figure** The 741 second stage prepared for small-signal analysis
This is used to determine the values of the parameters of the equivalent circuit.

**Input Resistance:** The resistance $R_{i2}$ is given by

$$R_{i2} = (\beta_{16} + 1)[r_{e16} + R_9 \parallel (\beta_{17} + 1)(r_{e17} + R_8)]$$

So, $R_{i2} = 4\text{M}\Omega$.

**Transconductance:** From the small-signal equivalent circuit model of the second stage, we can observe that,

$$G_{m2} = \frac{i_{c17}}{v_{i2}}$$
\[ i_{c17} = \frac{\alpha v_{b17}}{r_{e17} + R_8} \]
\[ v_{b17} = v_{i2} \frac{(R_9 \parallel R_{i17})}{(R_9 \parallel R_{i17}) + r_{e17}} \approx v_{i2} \]

- So, \( G_{m2} = 6.5 \, \text{mA/V} \)
- **Output Resistance**: output resistance of the second stage is given by,
  \[ R_{02} = (R_{013B} \parallel R_{017}) \]
- Where, \( R_{013B} = r_{e13} \), for 741 \( r_{e13} = 90.9 \, \text{k}\Omega \).
- Where, \( R_{017} = r_0[1 + g_m R_8] = 787 \, \text{k}\Omega \).
- Therefore, \( R_{02} = 81\,\text{k}\Omega \).
Output Stage
**Figure** The 741 output stage.
GAIN, FREQUENCY RESPONSE AND SLEW RATE OF 741

Small signal gain, frequency response, a simplified model, slew rate, relationship between $F_t$ and SR
SMALL SIGNAL GAIN
The overall small-signal gain can be found from the cascade of the equivalent circuits.

Load resistance \( R_L = 2 \, \text{k}\Omega \).

The overall gain can be expressed as,

\[
\frac{v_o}{v_i} = \frac{v_i}{v_i} \cdot \frac{v_{i2}}{v_i} \cdot \frac{v_{o2}}{v_{i2}} = -G_{m1} (R_{o1} || R_{i2}) (-G_{m2} R_{o2}) G_{vo3} \frac{R_L}{R_L + R_{out}}
\]

So, \( A_o = -476.1 \times (-526.5) \times 0.97 = 243,147 \, \text{V/V} \)
FREQUENCY RESPONSE
Figure: High frequency model of OP-AMP

Diagram of high frequency model of OP-AMP.
- Frequency response of the op-amp is the plot of its open loop gain versus frequency.
- The open loop gain changes with frequency.
- To plot the frequency response we need to refer high frequency model of OP-AMP.
- After a certain frequency the rolloff decreases after certain frequency.
- The capacitor is due to BJT used in the 741.
- The BJTs has parasitic capacitances so the capacitances is too small.
- So in order to reduces the effect of this parasitic capacitances the compensated capacitor is used in 741.
A SIMPLIFIED MODEL
In simplified model of 741, the high-gain second stage, with its feedback capacitance $C_C$ is modeled by an ideal integrator.

In this model, the gain of the second stage is assumed to be very large.

That’s why the output resistance of the input stage and the input resistance of the second stage have been omitted.

The output stage is assumed to be an ideal unity gain follower.

$$A(s) = \frac{V_o(s)}{V_i(s)} = \frac{G_{m1}}{sC_C}$$

$$A(j\omega) = \frac{G_{m1}}{j\omega C_C}$$
The magnitude of the gain becomes unity at $\omega = \omega_t$

Where, $\omega_t = \frac{G_m}{C_c}$

So, $f_t = \frac{\omega_t}{2\pi} \approx 1 MHz$

Where, $f_t$ is called unity gain frequency.

At $f >> f_{3dB}$, the gain falls off with a slope of 20dB/decade, just like an integrator.
Slew rate
Consider the unity-gain follower shown on previous slide.

10 volt step is applied at the input.

The entire value of the step signal will appear as a differential signal between the two input terminals.
From the circuit shown on previous slide, we see that, output voltage ramp with a slope of $2I/C_C$.

$$v_0(t) = \frac{2I}{C_C} t$$

So the slew rate is given by: $SR = \frac{2I}{C_C}$

For 741 $SR = 0.63 \text{ V/µs}$.
RELATIONSHIP BETWEEN $F_T$ AND SR
Relationship between $f_t$ and SR can be found by:

$$\omega_t = \frac{G_{m1}}{C_C} \quad SR = \frac{2I}{C_C}$$

As we know that $G_{m1} = \frac{\alpha}{2r_e} = \frac{1}{2r_e} \quad \& \quad r_e = \frac{V_T}{I}$

So, $G_{m1} = \frac{I}{2V_T}$

So, $\omega_t = \frac{I}{2C_C V_T}$

And we get, $\omega_t = \frac{SR}{4V_T}$

Finally we get, $f_t = \frac{SR}{8\pi V_T}$
ALL THE BEST FOR INTERNAL EXAMS