2014

Ajay Kumar Gautam

[VLSI TECHNOLOGY]

VLSI Technology for 3RD Year ECE/EEE Uttarakhand Technical University

Syllabus

UNIT 1

Introduction to VLSI Technology: Classification of ICs, Scale of integration, semiconductor and hybrid ICs Features of ICs,

CRYSTAL GROWTH: monolithic and hybrid ICs, crystal growth, Czochralski technique of crystal growth, wafer preparation and specifications, testing, measurements of parameters of crystals, Fabrication steps,

OXIDATION: Theory of growth of Silicon di oxide layer, calculation of SiO_2 thickness and oxidation kinetics, Dry wet and high pressure oxidation, plasma oxidation, properties of oxidation, defects induced due to oxidation.

UNIT 2

EPITAXIAL PROCESS: Epitaxy and its concept, Growth kinetics of epitaxy, epitaxial growth, Low-temperature epitaxy, Si-epitaxy- growth chemistry of Si epitaxial layer, auto-doping apparatus for epitaxial layer, apparatus for epitaxy, MBE system

DIFFUSION PROCESS: Diffusion models of solid, Fick's theory of diffusion, Solution of Fick`s law, diffusion parameters measurements schemes,

ION IMPLANTATION: Scattering phenomenon, range theory, channeling, implantation damage, ion-implantation systems, Annealing

UNIT 3
LITHOGRAPHY: photolithography and pattern transfer, Optical and non-optical lithography, electron, X-ray and ion-beam lithography, contact/proximity and projection printers, alignment. Photoresist and ETCHING: Types of photoresist, polymer and materials, Etching- Dry & Wet etching, basic regimes of plasma etching, reactive ion etching and its damages, lift-off, and sputter etching.

UNIT 4

METALLIZATION: Applications and choices, physical vapor deposition, patterning, problem areas.

VLSI PROCESS INTEGRATION: PMOS, NMOS and CMOS IC technology, MOS memory IC technology, bipolar IC fabrication.

UNIT 5

ASSEMBLY TECHNIQUE AND PACKAGING: Package types, packaging design consideration, VLSI assembly technologies.

YIELD AND RELIABILITY: Yield loss in VLSI, yield loss modeling, reliability requirements, accelerated testing.

SUGGESTED BOOKS:

1. **S.M. SZE/ VLSI Technology / M Hill. 2009/2nd Edition**
2. **S. K. Gandhi/VLSI Fabrication Principles/Wiley/2nd edition**
3. **S.A. Campbell / The Science and Engineering of Microelectronic Fabrication / Oxford 2008/2nd edition**
4. **Sedra & Smith/ Microelectronic Circuits 2004/Oxford/5th edition**
5. **James D. Plummer/ Silicon VLSI Technology: Fundamentals, Practice, and Modeling/Pearson/2nded**

Question Bank

UNIT I

Introduction to VLSI Technology

1) Explain basic differences between Bipolar and MOS Integrated Circuits. **[UTU 2010]**

2) What are the advantages of Integrated circuits over discrete component circuits? **[UTU 2010]**

3) Give the steps used in the fabrication of ICs in a block diagram representation. **[UTU 2010]**

Crystal Growth

4) What are the various types of the defects in crystal structure, explain. **[UTU 2012]**

5) List the key steps involved in obtaining pure Silicon. Explain with block diagram. **[UTU 2011]**

6) Discuss different steps in preparing wafers from the raw silicon with help of block diagram. **[UTU2012]**

7) How do you obtain MGS form pure silicon? Give all the reactions that take place during the process. **[UTU 2012]**

8) Describe Cz process in detail with neat diagram. What is the Pull Rate in CZ technique? How the Pull Rate is controlled during the CZ crystal growth process? **[UTU 2010], [UTU 2013]**

9) What is CZ method? Explain along with its advantages and disadvantages. **[UTU 2012]**

10) Explain CVD process. Discuss its application. **[UTU 2010]**

11) A silicon ingot with 0.5×10^{16} boron atoms/cm^3 is to be grown by Cz method. What should be the concentration of boron in the melt to obtain the required doping concentration? The segregation coefficient of the boron is 0.8. **[UTU 2012] , [UTU 2013]**

12) A boron-doped crystal is measured at its seed end with a four-probe of spacing 1 mm. The (V/I) reading is 10 ohms. What is the resistivity at seed end? **[UTU 2012]**

Oxidation

13) Why SiO_2 is an important component in electronics? **[UTU 2011]**

14) Explain the application of SiO_2 layer in IC fabrication. **[UTU 2012]**

15) Compare wet oxidation with dry oxidation. Why wet oxides are faster than dry oxides? **[UTU 2011]**

16) Why Oxidation is necessary in IC fabrication? Calculate the oxide thickness. Show that $\frac{x}{A/2} = \left[1 + \frac{t+\tau}{A^2/4B}\right]^{1/2} - 1$, reduces to $x = \frac{B}{A}(t+\tau)$ for short time and to $x = \sqrt{B(t+\tau)}$ for long time, where x = oxide thickness. **[UTU 2010]**

17) Explain diffusion controlled case and reaction controlled case with the help of Deal Groove Model. **[UTU 2012]**

18) Derive the linear rate equation and parabolic rate equation for Si oxidation process. **[UTU 2012]**

19) Calculate the oxidation time required for the thermal oxidation of 100 A and 5000 A thickness at 1000 ^{0}C. Note B = 5.2x10^5 A^2/min and B/A = 111 A/min. **[UTU 2013]**

20) Describe two most common method used to measuring thermal oxide thickness. **[UTU 2013]**

UNIT II

Epitaxial Process

21) What is the difference between pseudo homo epitaxy and hetero epitaxy? **[UTU 2013]**

22) What is Epitaxy? Discuss Molecular Beam Epitaxy technique in brief. What are the advantages of MBE over VPE? **[UPTU 2007]**

23) Explain MBE process in detail. **[UTU 2012]**

24) What do you mean by epitaxy? Explain vapor phase epitaxy with its basic transport process. **[UTU 2012]**

25) Explain the kinetics of Epitaxy. Calculate epitaxial layer thickness. What are the sources of silicon in VPE? **[UTU 2012]**

26) What do you mean by Reynolds number? How Reynolds number shows the flow of gas? **[UTU 2012]**

27) Why epitaxial layer of Si is necessary to grow? What are the functions of this layer in IC? **[UTU 2010]**

28) What is Autodoping? What are the disadvantages of Autodoping? How it can be minimized?

Diffusion Process

29) Derive the diffusion equation. How the depth of diffusion is controlled during diffusion process? Give the solution of Fick's Law? **[UTU 2010]**

30) If the measured phosphorus profile is represented by a Gaussian function with a diffusivity D = 2.3×10^{-13} atoms/cm^2, the measured surface dose is 10^{18} atoms/cm^2 and the measured junction depth is 1 μm at a surface concentration of 10^{15} atoms/cm^3. Calculate the diffusion time. **[UTU 2012]**

Ion Implantation

31) Describe a typical ion implanter. What are the advantages of ion implantation? **[UTU 2011]**

32) What is Ion Implantation? Explain the process with a neat diagram. **[UTU 2010]**

33) What do you mean by Annealing? Why it is required in IC fabrication process? **[UTU 2011]**

34) Compare ion implantation process with diffusion. **[UTU 2011]**

35) Explain the basic working principle of ion implantation process with all necessary equations. Compare between the diffusion and ion implantation process. **[UTU 2012]**

36) How the impurity concentration and junction depth are independently controlled in an ion implantation process? **[UTU 2013]**

37) State the final impurity distribution equation for two diffusion i.e., pre deposition followed by drive in diffusion. Give the examples of constant source and limited source diffusion. **[UTU 2013]**

UNIT III

Lithography

38) What do you mean by photo-resist? Explain various types of photo-resist. **[UTU 2012]**

39) List the defects in pattern transfer. **[UTU 2012]**

40) List all process steps of pattern transfer with diagram. **[UTU 2012]**

41) What are PR materials? Describe all types of PR. What are the properties of PR? **[UTU 2012]**

42) Explain proximity printing and projection printing & compare these two. **[UTU 2011]**

43) List and compare different types of lithography techniques. **[UPTU 2007]**

44) Explain ion beam lithography process. **[UTU 2011]**

45) What are the requirements of a photoresist? Which photoresist is preferred for better resolution and why? **[UPTU 2007], [UTU 2013]**

46) Describe ion beam lithography in brief. **[UPTU 2006]**

47) Describe various printing techniques in lithography. Which one is better and why?

48) What is the difference between positive and negative photoresist? Which photoresist is preferred for better resolution and why? **[UPTU 2006]**

49) List and explain all the steps of pattern transfer using photo lithography process. **[UTU 2011]**

50) Explain X-Ray lithography process. How will you calculate the blur? **[UTU 2012]**

51) What is X-Ray lithography? Describe advantages and problem areas associated with X-Ray lithography. **[UTU 2013]**

Etching

52) What is plasma? Draw an equivalent circuit for RF plasma discharge. **[UPTU 2006]**

53) Explain all properties of etchant. **[UTU 2011]**

54) What do you mean by etching process? Explain all the etching process in brief with neat diagram. **[UTU 2012]**

55) What is reactive ion etching? Describe its damages. **[UPTU 2006]**

56) Explain the kinetics of wet etching. How gold is etched? **[UTU 2012]**

57) Why higher degree of anisotropy is required in VLSI fabrication? **[UTU 2013]**

UNIT IV

Metallization

58) Explain the metallization and describe the problems associated with this process. Explain dc sputtering method of metallization. **[UTU 2011]**

59) How the thickness of deposited film is measured?

60) Why Metallization is required? What advantages and applications it provide the ICs?**[UTU 2010]**

61) What do you mean by junction spiking? Suggest some solutions to remove junction spiking effects. **[UTU 2013]**

62) What is electromigration; suggest some solutions to get rid of the electromigration problem. **[UTU 2013]**

VLSI Process Integration

63) With neat diagram explain fabrication process sequence for NMOS IC technology **[UPTU 2006]**

64) Why <100> orientation is preferred over <111> orientation for starting material in NMOS/CMOS IC fabrication. **[UPTU 2006]**

65) Explain CMOS inverter Voltage transfer characteristic with a neat diagram. Explain fabrication process for n-tub CMOS IC. **[UPTU 2006]**

66) Explain the various fabrication steps of NPN transistor with diagrams and brief explanation. **[UTU 2011]**

67) How a NPN transistor can be fabricated? Explain all the steps of fabrication. Also compare it with NMOS fabrication. **[UTU 2012]**

68) Illustrate with schematic block diagrams the process sequence of BJT process. Also discuss the function of the buried layer in BJT. [**UTU 2013]**

69) What do you mean by MOS Memory devices? What are its applications? Give complete fabrication steps. **[UTU 2013]**

70) Give the various fabrication steps of CMOS transistor using n well technique with diagrams and brief explanation. **[UTU 2011]**

71) What is the “hot electron problem” in NMOS IC? How it can be minimized?

72) What are the stored charge and the number of electrons on an MOS capacitor with an area of 4 μm^2, a dielectric of 200 $\overset{0}{A}$ thick SiO_2, and an applied voltage of 5V?

73) Describe various effects if the channel doping is either too low or too high in NMOS IC technology.

UNIT V

Assembly Technique and Packaging

74) Why packaging is required? Explain flip chip technology. **[UTU 2012]**

75) Write short note on package types and packaging design VLSI Technology. What is meant by DIP? Explain in brief. **[UTU 2011]**

76) Write a short note on VLSI assembly technologies. Describe the different VLSI assembly technologies. **[UTU 2011]**

77) How is packaging evaluated for VLSI design? Discuss the types of packaging design consideration. **[UTU 2013]**

Yield and Reliability

78) Write a detailed note on different yield loss mechanisms in VLSI. **[UTU 2011]**

79) Explain why modeling of yield loss mechanisms is required. Explain general model of yield loss mechanism and also explain accelerated testing in brief. **[UTU 2012], [UTU 2013]**

80) What do you mean by Yield in VLSI? How you can have the products with overall high Yiels? Explain the trade-offs also to achieve the high yield. **[UTU 2012]**

81) Explain the reliability in terms of VLSI technology. Explain how is accelerated testing performed? **[UTU 2013]**